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Enhanced voltage source converter control strategy for improved grid resilience: A 2DOF-PI approach

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ABSTRACT

This paper presents a control strategy for voltage source converters connected to weak grids. The proposed approach is based on slight modifications to the conventional vector current control strategy, including the use of two degrees of freedom proportional-integral controllers, with reference weighting factors, in the inner current loop and a proportional controller in the outer loop, resulting in the introduction of only three additional parameters. The paper analyses the effect of these additional design parameters on the robustness improvement and studies the limitations of the proposal, providing design steps to achieve given performance prescriptions such as speed response, noise amplification, delays and phase-locked loop bandwidth, and the ability to face weak grids. Simulations are conducted to evaluate the effectiveness of the proposed approach, which demonstrates that it is possible to achieve a more robust behaviour compared with the conventional vector current control strategy when facing weak grids.

1. Introduction

The increasing penetration of renewable energies has led to a widespread deployment of power electronics devices, specially Voltage Source Converters (VSC) [1,2]. In this regard, one of the most widely used control strategy for grid following converters is the Vector Current Control (VCC), which is based on the independent control of the two current components d and q in the synchronous reference frame (SRF), while the synchronization is realized by means of a Phase-Locked Loop (PLL) [3]. These current references are usually provided by an outer loop that controls the active power and voltage/reactive power. Despite its good behaviour in stiff grids, VCC presents stability problems when the VSC is connected to Weak Grids (WG), i.e., a Short-Circuit Ratio (SCR) < 3 [4,5]. Several studies have analysed this problem, focusing mainly on three parts of the control structure: (i) PLL, (ii) outer power loop and (iii) inner current loop.

The first group of studies analyses the effects of the PLL parameters over the VSC performance. In [6], their authors propose to reduce the PLL bandwidth for improving the overall system stability. In [7] it is proposed to design the PLL and the outer voltage regulator at the same time and also the use of an infinite artificial bus for the reference of the PLL measurements. In [8], the interactions between the PLL and the outer and inner control loops are studied and in [9] it is proposed a criterion for selecting a PLL's bandwidth to ensure the system stability. The power synchronization technique in [10–12] avoids the use of the PLL by emulating the behaviour of a synchronous machine, the voltage modulated direct power control in [13] requires neither the use of a PLL nor Park transformations while maintaining the VCC structure or in [14] authors propose to use a fixed frequency and an anti-windup mechanism to avoid the use of the PLL.

The second group focuses on the outer control loop. According to [15], it can be categorized into two categories: voltage disturbance feed-forward control [16], in which the current reference is directly computed from the measured voltage, and the power feedback control [17–19]. In [17], authors show the positive feedback introduced by the PLL and propose to reshape the converter output impedance in order to counteract it. In [18] the authors propose a lookup table to modify the PI parameters of the outer loop for different operating points and in [19] it is proposed the use of a feed-forward branch that estimates the reactive power needed as a function of active power demands.

The third group is focused on the inner current loop. In [20] it is studied the influence of the critical parameters of the current loop on the system stability. In [21] it is shown how to achieve stable inertia emulation by reducing the inner loop time constant. In [14], the authors analyse different instability sources and they propose a design method for minimizing the SCR level in which the VSC can operate.

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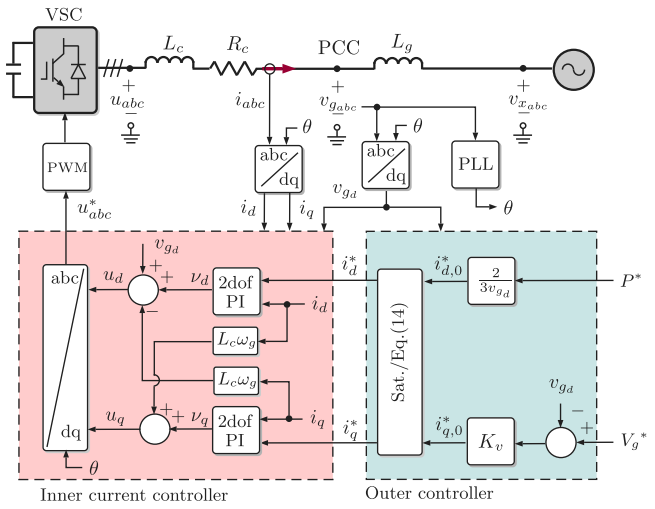

Fig. 1. Proposed control of a VSC connected to a WG.

The inner control loop uses feed-forward and decoupling terms for ensuring a decoupled control of both i_d and i_q currents, even in weak grids. However, the outer power control loops introduce a new voltage feedback, resulting in coupling between both loops [22]. This fact introduces new dynamics that are typically not considered when designing the controllers and analysing the stability [23,24]. Moreover, many approaches use a predefined formula for designing the inner current control loop PI controllers such as the Internal Model Control (IMC) method [25–28], which focuses on achieving a desired time-response under stiff grids. However, this does not guarantee a good performance under WG. Additionally, most stability studies based on the system's eigenvalues, simply analyse the influence of certain parameters on the system's stability but do not provide design procedures oriented towards weak grids [6,29,30].

In this work, the problems derived from the WG operation are addressed from two points of view: the control structure and the controller design method. On one hand, concerning the control structure, a cascaded-control strategy is proposed using a 2 degrees of freedom proportion integral (2DOF-PI) controller for the inner control loop and a proportional control for the outer loop, enhancing the VSC performance and robustness in WG environments. On the other hand, through a normalization procedure and an in-depth analytical analysis of the system, a design method based on the trade-off between time response, robustness against uncertainties, and the feedback channels derived when facing WG, voltage deviations, and the maximum supported delays is proposed. This design method translates the specifications into constraints on the controller parameters. With this design method, wider controller searching areas can be explored than, for instance, with the predefined IMC-based controller design techniques. The 2DOF-PI proposal includes two weighting factors that are directly related to the affordable grid weakness. In that sense, the use of weighting factors and a voltage proportional controller allows for enhancing the VSC performance and robustness in WG environments. Furthermore, the extra degrees of freedom allow for focusing on both the problems of guaranteeing a given nominal dynamics and a given robustness when facing weak grids.

In this work, subscript *abc* refers to a vector $x_{abc} = \begin{bmatrix} x_a & x_b & x_c \end{bmatrix}^T$ where x_a, x_b, x_c are the values that take the three phases of the variable x (in a balanced three-phase electrical system) and subscript dq a vector $x_{dq} = \begin{bmatrix} x_d & x_q \end{bmatrix}^T$, where x_d, x_q are the d and q components of x in a SRF with an angular velocity ω_g (grid frequency). Superscript "*" refers to reference signals, subscript "o" is used for operating points and Δx denotes an incremental variable such that $\Delta x = x - x_o$. $\mathbf{I}$ refers to the Identity matrix of the corresponding dimensions and $\mathbf{J}$ the rotation matrix

$$\mathbf{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}.$$

2. System description

Fig. 1 shows the model of a VSC connected to a weak transmission grid modelled by its Thevenin's equivalent, L_g and $v_{x_{abc}}$. For the grid impedance, it is assumed to be inductive given that high voltage ac (HVAC) transmission grids are considered, thus, the resistive component is neglected. However, lower X/R ratios favour the grid stability [31,32], therefore, considering only L_g represents the worst case. For the VSC, a Modular Multilevel Converter (MMC) is considered, which does not require an output filter. In Fig. 1, R_c and L_c represent the resistance and inductance of the VSC transformer, u_{abc} is the voltage at VSC terminals, $v_{g_{abc}}$ is the voltage at the PCC, and i_{abc} the current flowing from the VSC to the grid. S_r (> 0) is the rated power and V_N (> 0) the nominal voltage of the VSC (phase-to-ground peak value), which coincides with the grid nominal one.

The differential equations in the SRF that describes the dynamics of the VSC are

$$\frac{di_{dq}}{dt} = -\left(\frac{R_c}{L_c}\mathbf{I} + \omega_g \mathbf{J}\right) i_{dq} + \frac{1}{L_c}\left(u_{dq} - v_{g_{dq}}\right), \tag{1}$$

and the equations related to the grid

$$v_{g_{dq}} = L_g\left(\omega_g \mathbf{J}\, i_{dq} + \frac{di_{dq}}{dt}\right) + v_{x_{dq}}. \tag{2}$$

The instantaneous active and reactive powers P and Q exchanged with the AC WG are given by

$$S = \begin{bmatrix} P & Q \end{bmatrix}^T = \frac{3}{2}\begin{bmatrix} v_{g_{dq}} & \mathbf{J}^T v_{g_{dq}} \end{bmatrix} i_{dq}. \tag{3}$$

The amplitude of the rated current ($I_r > 0$, phase peak value) in the SRF of the VSC can be defined as

$$I_r = \frac{2\,S_r}{3\,V_N} \tag{4}$$

and the base impedance as

$$Z_b = \frac{V_N}{I_r} = \frac{3\,V_N^2}{2\,S_r}. \tag{5}$$

Finally, the stiffness of the grid is defined through the SCR, defined as the ratio between the short-circuit capacity of the grid at the PCC (S_{cc}) and the maximum possible power ($P_{\max}$) of the VSC, and it can be expressed as

$$\mathrm{SCR} = \frac{S_{cc}}{P_{\max}} = \frac{3}{2}\frac{V_N^2}{L_g\omega_g\,P_{\max}} = \frac{3}{2}\frac{V_N^2}{X_g\,P_{\max}}, \tag{6}$$

where the grid impedance is introduced as $X_g = L_g\,\omega_g$. In the case that the maximum achievable power in the VSC is $P_{\max} = S_r$, the nominal SCR can be expressed as a ratio of base and grid impedances as

$$\mathrm{SCR}_N = \frac{S_{cc}}{S_r} = \frac{3}{2}\frac{V_N^2}{L_g\omega_g\,S_r} = \frac{Z_b}{X_g}. \tag{7}$$

2.1. Conventional VCC strategy

The most common implementation for the conventional VCC is in the SRF. To synchronize the control signals with the AC grid, a PLL is used. When aligning the PCC voltage with the d-axis, it results in $v_{g_q} = 0$ and $v_{g_d} = V_g$, where V_g represents the grid voltage amplitude.

In the conventional VCC, control actions in the SRF u_{dq} are

$$u_{dq} = v_{g_{dq}} + L_c\,\omega_g\,\mathbf{J}\,i_{dq} + \nu_{dq}, \tag{8}$$

$$\nu_{dq} = K_p\,(i^*_{dq} - i_{dq}) + K_i\int (i^*_{dq} - i_{dq})\,dt. \tag{9}$$

They are composed of terms obtained from the PI controller (9), and feed-forward and decoupling terms (first two addends in (8)) to counteract the coupling between the d and q components of the current shown in (1). Thanks to this decoupling mechanism, two equal and decoupled systems are obtained, one for each channel (d and q). Considering a perfect decoupling, the two PI controllers are designed independently and with the same gains K_p, K_i. In this sense, design methods based on IMC reduce the design to a unique parameter α related to obtain a specific time-response in tracking current references. Attending to the IMC design method, PI gains are obtained as

$$K_p = \frac{L_c}{\alpha}, \qquad K_i = \frac{R_c}{\alpha}. \tag{10}$$

This method has been widely analysed in the design of PI controllers for current control [25–27,33] and leads to a decoupled first order closed loop dynamics under stiff grid conditions given by

$$\frac{di_d}{dt} = \frac{-1}{\alpha} i_d + \frac{1}{\alpha} i_d^*,$$
$$\frac{di_q}{dt} = \frac{-1}{\alpha} i_q + \frac{1}{\alpha} i_q^*.$$

In the sequel, a proposal for current control is presented, covering this method as a special case, and the limitations of this IMC method when facing weak grids will be shown.

3. Proposed approach

The conventional VCC strategy has been proven to be valid in stiff grids. However, it shows a poor behaviour in WG because the coupling between d and q axis as it will be seen in Section 4.2. As a result, the decoupling strategy cease to be valid so it is necessary to take into account the grid dynamics.

Therefore, the question arises as to whether it is possible to establish a control structure based on the VCC, with few design parameters that allows to operate VSCs in WG conditions, and to develop a design method for guaranteeing specifications in terms of time response, robustness against the feedback channels derived of the WG, high frequency behaviour, voltage deviations and maximum supported delays.

Fig. 1 shows the control proposal that is composed of an inner current control loop based on two PI controllers with Two Degrees Of Freedom (2DOF-PI), and an outer loop based on static functions that provides the current references for the inner current loop.

3.1. Inner current controller

For the inner current control loop the control actions u_{dq} are defined as

$$u_{dq} = v_{g_{dq}} + L_c \omega_g \mathbf{J} i_{dq} + v_{dq}, \tag{11a}$$

$$v_{dq} = K_p(b_{dq} i_{dq}^* - i_{dq}) + K_i \int (i_{dq}^* - i_{dq})\, dt, \tag{11b}$$

where the conventional feed-forward and decoupling terms are used, whereas the PI controllers include new tunable parameters

$$b_{dq} = \begin{bmatrix} b_d & 0 \\ 0 & b_q \end{bmatrix}$$

that weight the reference signals in the proportional term. As in conventional VCC, it is proposed to use the same parameters K_p, K_i for both 2DOF-PI controllers. Unlike the IMC approach, it is allowed the control parameters to be independently chosen, removing the constraint of being linked through α (see (10)).

In stiff grids, the feedforward terms in the controller are used to decouple the d and q channels, leading to two independent closed-loop transfer functions. Additionally, the integral term guarantees zero error in tracking current references. The performance (oscillatory behaviour, settling time, etc.) of these independent transfer functions is defined by the poles of the system, and they depend only on the parameters K_p and K_i. The new tunable parameters b_d and b_q only affect the zeros of the system, and with them, the overshoot against current reference changes can be reduced.

In weak grids the control actions affect the voltage $v_{g_{dq}}$, and, as it can be observed in the outer controller in Fig. 1, the changes in $v_{g_{dq}}$ modify the current references i_{dq}^*. A coupling between the d-q channels appears, and the conventional feedforward terms used for decoupling lose their effectiveness. In this sense, b_d and b_q help to dealing with the coupling derived from the weak grid in a similar way as it is done in some related works as [22]. In addition, since b_d and b_q can take values between 0 and 1, they can help to attenuate direct gain (if necessary) that appears in feedback through the weak grid. Note that these weighting factors do not affect the tracking error being integrated and, therefore, the guarantee of null steady state error is kept.

Moreover, two new parameters are introduced, serving as weighting factors in the PI control, thereby resulting in a 2DOF-PI control.

3.2. Outer controller

The current references are computed from the outer loop devoted to track the active power reference P^* and to limit the voltage deviations at the PCC. Therefore, from (3), assuming that the synchronization is maintained by the PLL, considering d-axis alignment w.r.t. the voltage v_g, and, with the aim of keeping the voltage deviations bounded between acceptable values, the current references are computed as

$$i_{d,0}^* = \frac{2\,P^*}{3\,v_{g_d}}, \tag{12}$$

$$i_{q,0}^* = K_v \left(V_g^* - v_{g_d} \right), \tag{13}$$

where $-S_r \le P^* \le S_r$, being P^* positive for power injection and negative for power absorption, $V_g^* = V_N$ is the reference value for the PCC voltage, and K_v is the design parameter of a proportional (P) controller.

Note that the active power controller (12) is based on inversion, i.e., computes the needed i_d current for the actually measured real voltage. As the current controller will track the received reference due to its integrator, the desired active power P^* will also be tracked without error in steady state. The voltage controller (13) is just a proportional controller (without integral term) that will not track the desired voltage in steady state, and the error depends on the value of the controller gain K_v. The previous explanations about tracking errors are true whenever the computed $i_{dq,0}^*$ values are sent directly to the current controllers. When the computed currents by (12) and (13) fulfil $\sqrt{{i_{d,0}^*}^2 + {i_{q,0}^*}^2} > Ir$, they must be decreased by a saturation procedure to guarantee $\sqrt{i_d^{*2} + i_q^{*2}} \le Ir$, where i_{dq}^* represents the altered version of $i_{dq,0}^*$ that is sent to the current controller to fulfil the limits (block named Sat. in Fig. 1). Then, to avoid over-currents, the references i_d^*, i_q^* are proposed to be limited as

$$i_q^* = \begin{cases} i_{q,0}^*, & \text{if} \quad -I_r \le i_{q,0}^* \le I_r \\ \text{sgn}(i_{q,0}^*)\, I_r, & \text{otherwise} \end{cases} \tag{14a}$$

$$i_d^* = \begin{cases} i_{d,0}^*, & \text{if } {i_{d,0}^*}^2 + i_q^{*2} \le I_r^2 \\ \text{sgn}(i_{d,0}^*) \sqrt{I_r^2 - i_q^{*2}}, & \text{otherwise} \end{cases} \tag{14b}$$

With this proposal, the scenarios outlined below can be observed and summarized in Fig. 2. Each scenario is defined, explaining the situations in which they occur, the finally demanded currents i_d^* and i_q^* sent to the current controller (see (11b)), and their relationship with the initially demanded currents by (12) and (13) before applying limitations (14a) and (14b).

(a) Stiff or weak grids when it can be reached the demanded currents $i_{d,0}^*$ and $i_{q,0}^*$ through (12) and (13) when they fulfil ${i_{d,0}^*}^2 + {i_{q,0}^*}^2 < I_r^2$. In this case,

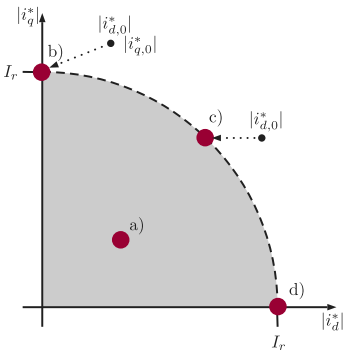

Fig. 2. Characterization of the different scenarios.

- $|i_d^*| < I_r$, $|i_q^*| < I_r$, and $i_d^{*2} + i_q^{*2} < I_r^2$.
- $i_q^* = i_{q,0}^*$ and $i_d^* = i_{d,0}^*$.

(b) Weak grids with high voltage drop that must be compensated demanding high currents higher than the rated one, i.e., $|i_{q,0}^*| > I_r$ in (13). In this case it is prioritized minimizing the error in tracking the demanded $i_{q,0}^*$ current over the demanded $i_{d,0}^*$ one to avoid large voltage deviations in such a way that

- $i_d^* = 0$ and $|i_q^*| = I_r$,
- $|i_q^*| < |i_{q,0}^*|$ and $i_d^* < |i_{d,0}^*|$.

(c) Weak grids when the power demanded is high, i.e., when for a given demanded q current $|i_{q,0}^*| < I_r$ in (13), the demanded d one through (12) fulfils ${i_{d,0}^*}^2 > I_r^2 - {i_{q,0}^*}^2$. In this case it is also prioritized $i_{q,0}^*$ over $i_{d,0}^*$, having

- $|i_q^*| < I_r$ and $i_d^{*2} = I_r^2 - i_q^{*2}$.
- $|i_q^*| = |i_{q,0}^*|$ and $|i_d^*| < |i_{d,0}^*|$.

(d) Stiff grids when the demanded power is the rated one and where the voltage in the grid is equal to the nominal one. In this case,

- $i_d^* = I_r$ and $i_q^* = 0$.
- $i_d^* = i_{d,0}^*$ and $i_q^* = i_{q,0}^*$.

With the proposed limitation, tracking the q axis current is preferred over tracking the d one when it is not possible to track both. Although this may sound contradictory, this option allows to achieve minimum power deviations in high demanding current situations during connection to weak grids. The fact is that preferring the track of q axis helps the converter to keep the voltage v_{gd} close to the nominal one, and that helps the power controller to ask for lower d currents that are closer to the achievable values, thus minimizing the power tracking error. On the other hand, as excessively voltage drop could cause disconnection of the VSC by protection mechanisms, the preference in tracking i_q, helps to maintain the VSC connected avoiding intermittent active power injection.

In the following section a detailed analysis is carried on demonstrating the goodness of the saturation proposal, being also compared to other alternatives that lead to poorer power tracking results and higher voltage drops at the PCC.

4. Analysis of the proposal

In this section the properties of the proposal in steady state, transient and high frequency behaviours are shown. In the transient behaviour the conditions for stability and robustness against measurement delays or PLL bandwidth, and the conditions to guarantee a given settling time under step changes are stated.

4.1. Steady state properties

In steady state, the grid branch fulfils

$$v_{g_{dq}} = L_g\,\omega_g\,\mathbf{J}\,i_{dq} + v_{x_{dq}}. \tag{15}$$

The grid voltage modulus is considered to be equal to the nominal voltage, i.e., $V_N = \sqrt{v_{x_d}^2 + v_{x_q}^2}$. In addition, in steady state, $i_q = i_q^*$ and, according to (13), i_q will be equal to

$$i_q = \begin{cases} K_v(V_N - v_{g_d}), & \text{if } |K_v(V_N - v_{g_d})| < I_r, \\ I_r, & \text{otherwise.} \end{cases} \tag{16}$$

Thus, for any P^* that is, i_d, the PCC voltage will be

$$v_{g_d} = \frac{-L_g\omega_g K_v V_N + \sqrt{V_N^2 - \left(L_g\omega_g i_d\right)^2}}{1 - L_g\omega_g K_v}. \tag{17}$$

It shows that v_{g_d} decreases as i_d increases (in absolute value). Thus, to state the maximum voltage deviation, the scenario (c) in which saturation applies on i_d^* is considered. It leads to

$$i_q = K_v(V_N - v_{g_d}), \quad i_d = \sigma\sqrt{I_r^2 - i_q^2}$$

where σ depends on power injection/absorption as

$$\sigma = \begin{cases} +1, & \text{if} \quad P^* > 0 \quad \text{(injection)} \\ -1, & \text{if} \quad P^* < 0 \quad \text{(absorption)} \end{cases} \tag{18}$$

Considering (5), the voltage in p.u. defined in (17) is

$$\frac{v_{g_d}}{V_N} = \frac{-X_g K_v + \sqrt{\left(1 - X_g K_v\right)^2 - \left(1 - 2X_g K_v\right)\left(\frac{X_g}{Z_b}\right)^2}}{1 - 2X_g K_v},$$

that must be understood as a function of voltage controller K_v, grid impedance X_g and base impedance Z_b. However, it can be rewritten as

$$\frac{v_{g_d}}{V_N} = \frac{-Z_b K_v + \sqrt{\left(\frac{Z_b}{X_g} - Z_b K_v\right)^2 - 1 + 2Z_b K_v \frac{X_g}{Z_b}}}{\frac{Z_b}{X_g} - 2Z_b K_v}, \tag{19}$$

where it is possible to identify the two independent and dimensionless parameters $Z_b K_v$ (that is, the constant gain K_v in p.u.) and $\frac{Z_b}{X_g}$ (that is, the inverse of grid impedance in p.u.) that define the voltage deviation. Similarly, the maximum (and derated) power in p.u. (given by $P_{\max} = v_{g_d}\,i_d$) can be read as

$$\frac{P_{\max}}{S_r} = \frac{v_{g_d}}{V_N}\sqrt{1 - \left(Z_b K_v\right)^2\left(1 - \frac{v_{g_d}}{V_N}\right)^2}, \tag{20}$$

where v_{g_d} must be understood as function (19).

Both voltage and power deviation depend on the grid impedance X_g and the parameter K_v. Fig. 3 shows that for a given controller value K_v, the higher the grid impedance, the higher the voltage deviation. The short circuit ratio equation in (6) shows that for higher values of X_g and $P_{\max}$ lower SCR are obtained. However, it can be observed in Fig. 3 (obtained from expression (20)) that higher X_g lead to lower $P_{\max}$ values. Furthermore, the curves exhibit asymptotic behaviour for negative $Z_b K_v$ values. Therefore, high negative values do not yield any benefits in terms of steady state operation point. For that reason, it is not clear that supporting higher X_g values is equivalent to supporting weaker grids in the sense of SCR. It will be focused later on this issue in the examples, but it will mainly be assumed the hypothesis that achieving higher supportable X_g values leads to lower SCR values.

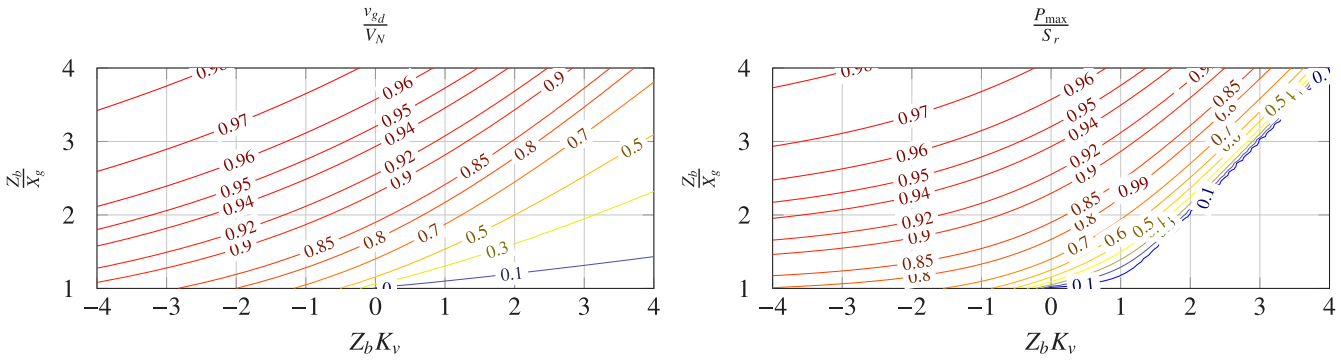

Fig. 3. Voltage (left) and P_{max} (right) levels at PCC as a function of $\frac{Z_b}{X_g}$ and $Z_b K_v$.

Fig. A.19 also shows in dashed lines the steady state values for voltage and power for an alternative saturation mechanism consisting on preferring tracking the i_d current over the i_q one (detailed in (A.1)). This alternative, although it may sound appropriate to guarantee a high power injection, leads to poorer results in both voltage and power. The reason is that higher voltage drops imply demanding higher i_d currents that, after saturation, lead to higher power error than the proposed approach (14). In other words, the proposed approach (14) leads to face weaker grids than the alternative approach (A.1) of preferring tracking the i_d current. The alternative saturation mechanism as well as the expressions for steady state that demonstrate this fact are detailed in Appendix.

4.2. Properties of the dynamic behaviour

Many studies [23,24] analyse the system stability considering the dynamics of the inner current control loop from i^*_{dq} to i_{dq}:

$$i_{dq}(s) = \boldsymbol{\Phi}^N(s) i^*_{dq}(s) = \begin{bmatrix} \phi^N_{1,1}(s) & 0 \\ 0 & \phi^N_{2,2}(s) \end{bmatrix} i^*_{dq}(s) \tag{21}$$

$$\phi^N_{1,1}(s) = \frac{b_d K_p s + K_i}{L_c s^2 + (K_p + R_c)s + K_i}, \quad \phi^N_{2,2}(s) = \frac{b_q K_p s + K_i}{L_c s^2 + (K_p + R_c)s + K_i}.$$

where the transfer function matrix $\boldsymbol{\Phi}^N(s)$ is[1]

$$\boldsymbol{\Phi}^N(s) = \left(\mathbf{I} - G_c\left(C_d - C_y\right)\right)^{-1} G_c C_r, \tag{22}$$

Non-diagonal elements are null so both current loops are decoupled, regardless of the grid stiffness. However, when controlling the power, these elements are not zero as demonstrated next.

Due to (12), leading to a non-linear dynamic behaviour, a small-signal analysis is developed in which (12) and (13) are linearized around an operation point ($V_{g,o}$, P^*_o).

$$\begin{bmatrix} \Delta i^*_d \\ \Delta i^*_q \end{bmatrix} = \underbrace{H_S \begin{bmatrix} \Delta P^* \\ \Delta V^*_g \end{bmatrix}}_{i^{*S}_{dq}} + \underbrace{H_V \begin{bmatrix} \Delta v_{g_d} \\ \Delta v_{g_q} \end{bmatrix}}_{i^{*V}_{dq}} \tag{23}$$

where H_S and H_V are static matrices defined as

$$H_S = \begin{bmatrix} \frac{2}{3V_{g_o}} & 0 \\ 0 & K_v \end{bmatrix}, \qquad H_V = \begin{bmatrix} \frac{-2P^*_o}{3V^2_{g_o}} & 0 \\ -K_v & 0 \end{bmatrix}. \tag{24}$$

H_V indicates a loop through v_g that may produce instabilities, and its gain depends on the exchanged power at the operation point. For analysing the full operation of the VSC, the two worst cases have been studied, i.e., $|P^*_o| = S_r$ for injection and absorption, what it is denoted through $P^*_o = \sigma S_r$. The PCC voltage at the operation point

[1] The Laplace's complex variable dependence has been omitted for brevity.

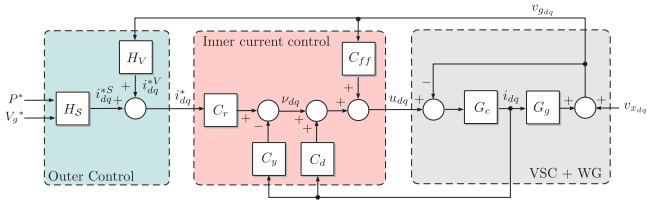

Fig. 4. Block diagram of the control approach with 2DOF PIs.

V_{g_o} depends on the P^*_o as shown in (17). However, it is considered that $V_{g_o} = V_N$ because it allows us to derive tractable expressions that help to understand the limitations of the proposal. This is a reasonable assumption as it will be shown in the Simulation results section. With this,

$$H_S = \begin{bmatrix} \frac{2}{3V_N} & 0 \\ 0 & K_v \end{bmatrix}, \qquad H_V = \begin{bmatrix} -\frac{\sigma}{Z_b} & 0 \\ -K_v & 0 \end{bmatrix}. \tag{25}$$

With these definitions, the block diagram in Fig. 4 can be derived, in which the transfer function matrices that represent the different blocks are

$$G_c(s) = \frac{\frac{1}{L_c}}{s^2 + 2\frac{R_c}{L_c}s + \omega_g^2 + \frac{R_c^2}{L_c^2}}\left[(s + \frac{R_c}{L_c})\mathbf{I} - \omega_g \mathbf{J}\right],$$

$$G_g(s) = L_g\,(s\,\mathbf{I} + \omega_g\,\mathbf{J}), \quad C_{ff} = \mathbf{I}, \quad C_d = L_c\,\omega_g\,\mathbf{J},$$

$$C_r(s) = \left(b_{dq}\,K_p + \frac{K_i}{s}\right)\mathbf{I}, \quad C_y(s) = \left(K_p + \frac{K_i}{s}\right)\mathbf{I}.$$

where

$$v_{g_{dq}}(s) = G_g(s)\,i_{dq}(s) + v_{x_{dq}}(s),$$
$$i_{dq}(s) = G_c(s)\left(u_{dq}(s) - v_{g_{dq}}(s)\right),$$
$$u_{dq}(s) = C_r(s)\,i^*_{dq}(s) + \left(C_d - C_y(s)\right)\,i_{dq}(s) + C_{ff}\,v_{g_{dq}}(s).$$

As H_S is an static matrix and it is out of the closed-loop, it does not affect the stability analysis. Therefore, the dynamics from i^{*S}_{dq} to i_{dq} is represented as

$$i_{dq}(s) = \boldsymbol{\Phi}(s) i^{*S}_{dq}(s) = \begin{bmatrix} \phi_{1,1}(s) & \phi_{1,2}(s) \\ \phi_{2,1}(s) & \phi_{2,2}(s) \end{bmatrix} i^{*S}_{dq}(s) \tag{26}$$

where the transfer function matrix $\boldsymbol{\Phi}(s)$ is

$$\boldsymbol{\Phi}(s) = \left(\mathbf{I} - G_c\left(C_d - C_y + C_r H_V G_g\right)\right)^{-1} G_c C_r, \tag{27}$$

and it depends on the VSC and grid parameters S_r, V_N, L_c, R_c, L_g, ω_g and on controller parameters K_p, K_i, K_v, b_d, b_q. In order to get tractable expressions, first, new dimensionless controller gains (denoted with "′") are defined as

$$K'_p = \frac{1}{R_c}K_p, \quad K'_i = \frac{L_c}{R_c^2}K_i, \quad K'_v = \frac{Z_b\,L_c\,\omega_g}{R_c}K_v, \tag{28}$$

$$\phi'_{1,1}(s') = \frac{\left(b_d K'_p s' + K'_i\right)\left(s'^2 + \left(\left(1 - b_q \frac{K'_v}{\mathrm{GS}}\right) K'_p + 1\right) s' + \left(1 - \frac{K'_v}{\mathrm{GS}}\right) K'_i\right)}{\left(s'^2 + \left(K'_p + 1\right) s' + K'_i\right)\left(\left(1 + b_d \frac{\sigma K'_p}{\mathrm{GS}}\right) s'^2 + \left(\left(1 - b_q \frac{K'_v}{\mathrm{GS}}\right) K'_p + 1 + \frac{\sigma K'_i}{\mathrm{GS}}\right) s' + \left(1 - \frac{K'_v}{\mathrm{GS}}\right) K'_i\right)} \tag{30a}$$

$$\phi'_{1,2}(s') = \frac{\frac{\sigma \omega'_g}{\mathrm{GS}}\left(b_d K'_p s' + K'_i\right)\left(b_q K'_p s' + K'_i\right)}{\left(s'^2 + \left(K'_p + 1\right) s' + K'_i\right)\left(\left(1 + b_d \frac{\sigma K'_p}{\mathrm{GS}}\right) s'^2 + \left(\left(1 - b_q \frac{K'_v}{\mathrm{GS}}\right) K'_p + 1 + \frac{\sigma K'_i}{\mathrm{GS}}\right) s' + \left(1 - \frac{K'_v}{\mathrm{GS}}\right) K'_i\right)} \tag{30b}$$

$$\phi'_{2,1}(s') = \frac{-\frac{K'_v}{\mathrm{GS}\omega'_g} s'\left(b_d K'_p s' + K'_i\right)\left(b_q K'_p s' + K'_i\right)}{\left(s'^2 + \left(K'_p + 1\right) s' + K'_i\right)\left(\left(1 + b_d \frac{\sigma K'_p}{\mathrm{GS}}\right) s'^2 + \left(\left(1 - b_q \frac{K'_v}{\mathrm{GS}}\right) K'_p + 1 + \frac{\sigma K'_i}{\mathrm{GS}}\right) s' + \left(1 - \frac{K'_v}{\mathrm{GS}}\right) K'_i\right)} \tag{30c}$$

$$\phi'_{2,2}(s') = \frac{\left(b_q K'_p s' + K'_i\right)\left(\left(1 + b_d \frac{\sigma K'_p}{\mathrm{GS}}\right) s'^2 + \left(K'_p + 1 + \frac{\sigma K'_i}{\mathrm{GS}}\right) s' + K'_i\right)}{\left(s'^2 + \left(K'_p + 1\right) s' + K'_i\right)\left(\left(1 + b_d \frac{\sigma K'_p}{\mathrm{GS}}\right) s'^2 + \left(\left(1 - b_q \frac{K'_v}{\mathrm{GS}}\right) K'_p + 1 + \frac{\sigma K'_i}{\mathrm{GS}}\right) s' + \left(1 - \frac{K'_v}{\mathrm{GS}}\right) K'_i\right)} \tag{30d}$$

a new Laplace variable s' leading to time units in relative terms w.r.t. the time constant of the system ($\frac{L_c}{R_c}$ [s]) as

$$s' = \frac{L_c}{R_c} s$$

that also leads to a dimensionless grid frequency value as

$$\omega'_g = \frac{L_c}{R_c} \omega_g.$$

Finally, a new dimensionless grid stiffness metric for nominal conditions is defined as

$$\mathrm{GS} = \frac{L_c}{R_c} \frac{Z_b}{L_g} = \frac{L_c}{R_c} \omega_g \, \mathrm{SCR}_N. \tag{29}$$

If it is applied the following change of variables in (27)

$$K_p = R_c K'_p, \quad K_i = \frac{R_c^2}{L_c} K'_i, \quad L_g = \frac{Z_b}{\mathrm{GS}} \frac{L_c}{R_c},$$
$$\omega_g = \frac{R_c}{L_c} \omega'_g, \quad s = \frac{R_c}{L_c} s', \quad K_v = \frac{1}{Z_b \omega_g} \frac{R_c}{L_c} K'_v.$$

the transfer functions $\phi'_{1,1}$, $\phi'_{1,2}$, $\phi'_{2,1}$, $\phi'_{2,2}$ in (30) are obtained, where the superscript "′" denotes those transfer functions in this new dimensionless frame. These transfer functions only depend on the normalized parameters of the controller (K'_p, K'_i, K'_v, b_d, b_q), the GS and ω'_g. From these expressions, it can be noticed (in terms $\phi'_{1,2}(s')$ and $\phi'_{2,1}(s')$) that there is a coupling effect that increases for weaker grids (i.e., for lower GS values).

Note that, in stiff grid nominal conditions, i.e., for $L_g \to 0$, (30) reduces to

$$\boldsymbol{\Phi}'^N(s') = \begin{bmatrix} \phi'^N_{1,1}(s') & 0 \\ 0 & \phi'^N_{2,2}(s') \end{bmatrix} \tag{31}$$

$$\phi'^N_{1,1}(s') = \frac{b_d K'_p s' + K'_i}{s'^2 + (K'_p + 1)s + K'_i}, \quad \phi'^N_{2,2}(s') = \frac{b_q K'_p s' + K'_i}{s'^2 + (K'_p + 1)s + K'_i}.$$

which is the same as (21). Hence, current and power control exhibit the same stability characteristics in strong grids. However, they notably differ in the case of weak grids. The zeros and poles are, respectively

$$z = \left\{ \frac{-K'_i}{b_d K'_p}, \frac{-K'_i}{b_q K'_p} \right\}, \tag{32}$$

$$p = -\frac{1}{2}(K'_p + 1) \pm \sqrt{\frac{(K'_p + 1)^2}{4} - K'_i} \tag{33}$$

It must be noticed that $\phi'^N_{1,1}(s')$ and $\phi'^N_{2,2}(s')$ have unitary static gain and low pass filter behaviour. A necessary condition to avoid poles with null or positive real part is that all the coefficients of the polynomial of the denominator are positive, i.e.,

$$K'_p + 1 > 0, \qquad K'_i > 0.$$

The behaviour will be oscillatory if

$$K'_i > (K'_p + 1)^2/4$$

and, in that case, the damping of the poles will be

$$\xi = \frac{K'_p + 1}{2\sqrt{K'_i}}. \tag{34}$$

In the case that $K'_i \leq (K'_p + 1)^2/4$, the poles will be real. Furthermore, if b_d and b_q fulfil

$$\{b_d, b_q\} < \frac{2\,K'_i}{K'_p(K'_p + 1)},$$

the zeros of the system will not be dominant, and, therefore, there will not be high overshoot due to zeros.

In the sequel, this analysis of the dynamic behaviour will be used to obtain: i) the stability limits in terms of the controller gains and the weakness of the grid, ii) the maximum delay associated to the measurement system plus PLL that can be supported, and (iii) expressions that allow us to assess speed of the time response.

4.2.1. Stability limits due to grid weakness

In order to obtain the conditions to guarantee the stability of the controlled system when facing weak grids, the focus should be on the denominator of transfer function (30) that contains the product of two polynomials. The first one is the same than in the stiff grid case, leading to poles (33), and the second one is a more involved polynomial including more controller parameters. Attending Descartes' rule of signs, a necessary and sufficient condition to have stable poles (i.e., with negative real part) is that the coefficients of that polynomial are all positive, i.e.,

$$1 + b_d \frac{\sigma K'_p}{\mathrm{GS}} > 0, \tag{35a}$$

$$\left(1 - b_q \frac{K'_v}{\mathrm{GS}}\right) K'_p + 1 + \frac{\sigma K'_i}{\mathrm{GS}} > 0, \tag{35b}$$

$$\left(1 - \frac{K'_v}{\mathrm{GS}}\right) K_i > 0. \tag{35c}$$

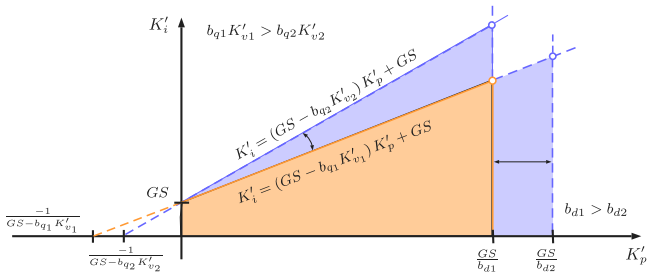

Fig. 5. Effect of the controller parameters on the feasibility regions.

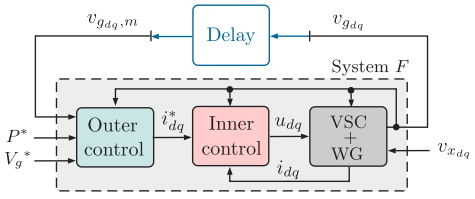

Fig. 6. Block diagram of the control approach with 2DOF PIs.

It can be seen that the added degrees of freedom through the weighting factors b_d, b_q and K_v are directly related to the stability of the system under weak grids.

From these conditions, it can be stated that, for some given controller parameters, the weaker grid that can be supported is given by

$$\mathrm{GS}_{\min} = \max\left\{ b_d K'_p,\ \frac{b_q K'_v K'_p + K'_i}{K'_p + 1},\ K'_v \right\} \tag{36}$$

where σ has been considered to face the worst case scenario (absorption in this case, i.e., $\sigma = -1$). With this value, and considering the GS definition in (29), it can be obtained, for a given controller, which is the highest admissible inductance before destabilizing, being

$$L^{GS}_{g,\max} = \frac{L_c}{R_c}\frac{Z_b}{\mathrm{GS}_{\min}}. \tag{37}$$

As can be seen, GS_{min} depends on the absorpted/injected power by the VSC. For positive values of the design parameters K_p, K_i (as it is usual), it is easy to demonstrate that the most restrictive stability condition is achieved for power absorption ($P^* < 0$). The limits established in (35) define feasibility regions, which depends on the controller parameters. Thus, by the use of the new parameters of the proposal (b_d, b_q, K_v) in addition to those of conventional VCC strategy (K_p, K_i), there is the capacity to modify the feasibility regions in such a way that, for the same controller (defined by K'_p, K'_i gains), weaker grids can be addressed, or from another point of view, for the same weakness (same value of GS_{min}), better performance can be achieved.

Fig. 5 shows graphically the feasibility regions and the effect of the parameters of the controller on the limits of those regions. As it can be observed, for positive values of K'_p and K'_i, two limits define these feasibility regions. On one hand, there is a vertical limit defined by $K'_p < \frac{\mathrm{GS}}{b_d}$. Thus, for a specific GS, the feasibility region can be expanded by reducing the value of b_d. On the other hand, there is a limit defined by $K'_i < (\mathrm{GS} - b_q K'_v)\,K'_p + \mathrm{GS}$, representing a line with a slope of $\mathrm{GS} - b_q K'_v$. Hence, for a particular GS, and assuming $K'_v < 0$, the feasibility region expands for higher absolute values of the product $b_q K'_v$. This graph can also be interpreted as follows: for the same controller (K'_p, K'_i), lower values for b_d or, lower values for the product $b_q K_v$ (assuming $K'_v < 0$) lead to lower values of $\mathrm{GS}_{\min}$.

4.2.2. Stability limits due to PLL or delays

In weaker grids, voltage deviations tend to be larger than in strong grids with high SCRs. Moreover, weaker grids are also more prone to experiencing severe voltage distortions in the case of unbalanced or non-linear loads. Given that the control is carried out in a synchronous reference frame, obtaining a non-distorted grid phase angle for the *abc* to *dq* transformations is crucial. In this context, several studies have proposed enhanced control algorithms based of Adaptive Filter Second-Order Generalized Integrator Frequency-Locked Loop (AF SOGI-FLL), Weighted Least Squares Estimations Phase Locked Loop (WLSE), Moving Average Filter Phase Locked-Loop (MAF), Cascaded Delayed Signal Cancellation PLL (CDSC-PLL) or filters with multi-resonant harmonic compensators [34,35]. In general terms, these approaches involve incorporating filters to eliminate high frequency harmonics from the measurements and lowering the PLL bandwidth, which introduce a delay in the measurement signals.

To analyse the effect of the filters and PLL on the closed-loop dynamics when used under weak grids, the focus is on the new feedback WG related channel through H_V, i.e., the time delay effect introduced through the measurement channel of v_{g_d} as shown in Fig. 6. and, to analyse its impact, the Generalized Nyquist Criteria [36] can be used. In this case, the open-loop system to be analysed is the transfer function that describes the relationship between the measured grid voltage $v_{g_{dq},m}$ and the resulting grid voltage $v_{g_{dq}}$, that is

$$v_{g_{dq}} = F(s)\, v_{g_{dq},m}, \quad F(s) = G_g(s)\boldsymbol{\Phi}^N(s)H_V(s), \tag{38}$$

being

$$F(s) = \begin{bmatrix} -\sigma\frac{L_g}{Z_b}\, s\, \phi^N_{1,1}(s) + X_g\, \phi^N_{2,2}(s)\, K_v & 0 \\ -\sigma\frac{X_g}{Z_b}\, \phi^N_{1,1}(s) - L_g\, s\, \phi^N_{2,2}(s)\, K_v & 0 \end{bmatrix}, \tag{39}$$

Due to the column-like form of matrix $F(s)$, the eigenvalues (denoted by $\lambda(s)$) of $-F(s)$ are[2]

$$\lambda(s) = \{0, -F_{1,1}(s)\}$$

i.e., zero, and the element (1,1) of matrix $-F(s)$. Therefore, only $\lambda(j,\omega) = -F_{1,1}(j,\omega)$ needs to be analysed in the complex plane to assess stability. If the aforementioned dimensionless procedure is applied, $\lambda(s)$ can be expressed as

$$\begin{aligned} \lambda(s') &= \frac{-1}{\mathrm{GS}}(-\sigma\, s'\, \phi'^N_{1,1}(s') + K'_v\, \phi'^N_{2,2}(s')) \\ &= \frac{\frac{1}{\mathrm{GS}}\left(\sigma\, b_d\, K'_p\, s'^2 + (\sigma K_i - b_q K'_v K'_p)s' - K'_i K'_v\right)}{s'^2 + (K'_p + 1)s' + K'_i} \end{aligned} \tag{40}$$

Attending the Generalized Nyquist Criterion, and assuming that $\lambda(s')$ is stable (as the poles of $\lambda(s')$ are the ones obtained in the nominal closed loop system, designed to be stable), the necessary conditions for stability are that

- for any frequency ω' such that $|\lambda(j\omega')| = 1$, the phase must fulfil $-\pi < \arg(\lambda(j\omega')) < \pi$. That frequency is called gain cross over frequency and is denoted by ω'_{gc}. Robustness metrics at that frequency ω'_{gc} as the phase margin PM (the amount of phase that can be added at that frequency before destabilizing the loop, i.e., $e^{-j\mathrm{PM}}\lambda(j\omega'_{gc}) = -1$) and the delay margin DM (the case where the phase margin is achieved by means of a pure delay, leading to $\mathrm{DM}' = \frac{\mathrm{PM}}{\omega'_{gc}}$) are obtained.
- for any frequency ω' such that $\arg(\lambda(j\omega')) = -\pi$ (i.e., when the frequency response is just a real negative value), the frequency response must fulfil $-1 < (\lambda(j\omega'))$. That frequency is called phase cross over frequency and is denoted by ω'_{pc}. The robustness metric gain margin GM at that frequency ω'_{pc} can be obtained as the amount of gain that can be added at that frequency before destabilizing the loop, i.e., ϕ such that $\lambda(j\omega'_{pc})\,\mathrm{GM} = -1$

[2] Note that the Nyquist criteria predicts for a negative feedback of the closed loop. As in this case, the block diagram includes a positive feedback, The sign of the transfer function being fed back is changed.

Attending (40) there is a transfer function $\lambda(s')$ with both finite static and direct gain, leading to

$$\lambda(0) = \frac{-K'_v}{\mathrm{GS}}, \quad \lambda(\infty) = \sigma \frac{b_d\, K'_p}{\mathrm{GS}}$$

where it must be considered both cases $\sigma = 1$ and $\sigma = -1$ (i.e., injection and absorption). Therefore, a necessary condition to avoid closed loop instabilities (attending to the gain margin criteria) is that

$$-1 < \frac{-K'_v}{\mathrm{GS}}, \quad -1 < \frac{b_d\, K'_p}{\mathrm{GS}}, \quad -1 < \frac{-b_d\, K'_p}{\mathrm{GS}}.$$

Note that as $K'_p > 0$, constraint $-1 < \frac{-b_d\, K'_p}{\mathrm{GS}}$ expressed for $\sigma = -1$ (i.e., absorption) is more critical than $-1 < \frac{b_d\, K'_p}{\mathrm{GS}}$. Note also that these conditions coincide with conditions (35) obtained from the analysis of the closed loop poles. On the other hand, condition $-1 < \frac{-K'_v}{\mathrm{GS}}$, if K_v is selected to be negative, does not impose any critical limitation.

The exact expression for the phase and delay margin is hard to obtain in this system, but it can be stated some limits to avoid delay problems if it is assured that the Nyquist plot does not intersect the unitary circle, i.e., $|\lambda(j\,\omega')| < 1$ for any ω'. The first necessary (but not sufficient) condition to avoid that is that

$$-1 < \lambda(j\,0) < 1, \quad -1 < \lambda(j\,\infty) < 1,$$

leading to

$$-1 < \frac{-K'_v}{\mathrm{GS}} < 1, \quad -1 < \frac{b_d\, K'_p}{\mathrm{GS}} < 1, \quad -1 < \frac{-b_d\, K'_p}{\mathrm{GS}} < 1.$$

These conditions coincide with the ones obtained to assure closed loop stability or can be derived from them except the new condition

$$K'_v > -\mathrm{GS}. \tag{41}$$

The second one is that the highest frequency response amplitude of $\lambda(j\,\omega')$ is also below one, i.e.,

$$\|\lambda(j\,\omega')\|_\infty < 1. \tag{42}$$

As this condition is hard to express analytically, it can be at least stated that this will be more probable to happen if the controller poles have enough damping, for instance, $\xi > 0.7$ in (34) and b_d close to zero (as $\lambda(j\,\infty)$ is proportional to it, see (40)).

In Fig. 7, the Nyquist diagram of $\lambda(s')$ is shown for three different controllers N1, N2 and N3. These controllers have the same K'_p and b_d values but different K'_i and K'_v values ($K'_{i_3} = K'_{i_1} < K'_{i_2}$ and $|K'_{v_1}| = |K'_{v_2}| < |K'_{v_3}|$). For a specific GS, since the three controllers have the same K'_p and b_d, $\lambda(\infty)$ is the same point for all three controllers and is located inside the unit circle. Regarding $\lambda(0)$, for controller N3, $K'_v < -\mathrm{GS}$ (i.e., condition (41) is not met), and thus, $\lambda(s')$ intersects the unit circle at a certain frequency ω'_{gc_3}, resulting in a phase margin PM_3 and a delay margin $\mathrm{DM3}' = \frac{\mathrm{PM}_3}{\omega'_{gc_3}}$. For controllers N1 and N2, $K'_v > -\mathrm{GS}$, which is a necessary but not sufficient condition to remain inside the unit circle. Therefore, as stated before, higher values of K'_i (i.e., lower damping) bring $\lambda(s')$ closer to intersecting the unit circle. In the graph, $K'_{i_1} < K'_{i_2}$ and it is shown that controller N1 remains inside the unit circle while controller N2 intersects it at a certain frequency ω'_{gc_2}, resulting in a phase margin PM_2 and a delay margin $\mathrm{DM}'_2 = \frac{\mathrm{PM}_2}{\omega'_{gc_2}}$. Here, the importance of the value $\frac{K'_v}{\mathrm{GS}}$ and the oscillatory nature of the closed-loop system (expressed with different K'_i values) in avoiding delay problems is highlighted.

4.2.3. Time response performance

For evaluating the speed response, one has on one hand the poles (33) of the system, that allow us to predict, for instance, the characteristic settling time[3] under disturbances, assuming complex poles, i.e., when the closed loop poles have imaginary part, leading to[4]

$$t'_{s,dist} = \frac{8}{K'_p + 1}. \tag{43}$$

In order to evaluate clearly the speed response when tracking power references, the use of the cumulative error when tracking current reference step changes in d axis is proposed. Thus, the normalized integral of the error $\mathrm{IE}' = \lim_{s'\to 0}(1 - \phi'_{1,1}(s'))\,\frac{1}{s'}$ is

$$\mathrm{IE}' = \frac{K'_p\,(1 - b_d) + 1 - \frac{1}{\mathrm{GS}}\left(K'_v\left(K'_p\,(1 - b_d) + 1\right) - \sigma\, K'_i\right)}{K'_i\left(1 - \frac{K'_v}{\mathrm{GS}}\right)}, \tag{44}$$

If the system has a low oscillatory behaviour, the normalized settling time can be approximated as

$$t'_s \approx 4\,\mathrm{IE}'. \tag{45}$$

In addition, the sensitivity of (44) w.r.t. the GS can be derived leading to

$$\frac{\partial \mathrm{IE}'}{\partial \mathrm{GS}} = \frac{-\sigma}{(K'_v - \mathrm{GS})^2}, \tag{46}$$

where it can be seen that a higher K'_v in absolute value has a benefit on keeping the dynamic behaviour for the nominal system (in terms of IE′) even in WG conditions. Therefore, parameter K'_v has an effect on achieving a given robustness in the closed loop behaviour. Note that, in stiff conditions, (45) reduces to

$$t'_s \approx 4\,\frac{K'_p\,(1 - b_d) + 1}{K'_i} \tag{47}$$

4.2.4. Coupling effects due to grid weakness

From the analysis of the transfer function $\Phi(s)$ in (27), one has the crossed elements shown in (30b) and (30c) that can be rewritten as

$$\phi'_{1,2}(s') = \frac{\frac{\sigma\omega'_g}{\mathrm{GS}}\left(b_d K'_p s' + K'_i\right)\left(b_q K'_p s' + K'_i\right)}{d(s)} \tag{48}$$

$$\phi'_{2,1}(s') = \frac{-\frac{K'_v}{\mathrm{GS}\omega'_g}\, s'\left(b_d K'_p s' + K'_i\right)\left(b_q K'_p s' + K'_i\right)}{d(s)} \tag{49}$$

being $d(s)$ the common denominator, and the following facts can be observed:

- both elements are higher as the grid weakness is larger, as both are proportional to $\frac{1}{\mathrm{GS}}$,

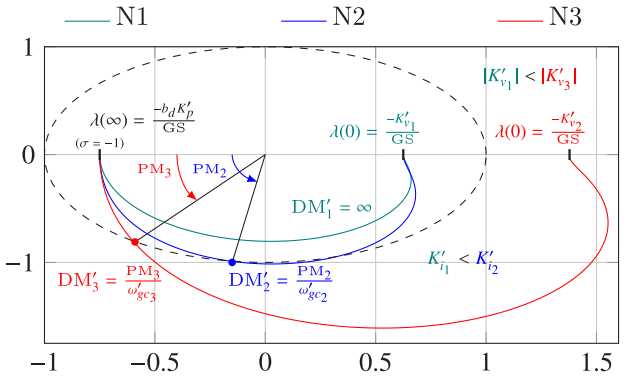

Fig. 7. Nyquist diagram of $\lambda(s')$ for different K'_v and K'_i, assuming $K'_v < 0$ and $\sigma = -1$ (absorption).

[3] In this work, the settling time is referred to the time in achieving the 98% of the steady state constant value of the corresponding variable.

[4] Note that the relationships between normalized time t' and time in seconds t is given by $t = \frac{L_c}{R_c}\, t'$.

- $\phi'_{2,1}(s')$ has a zero in the origin (element s' in the numerator), showing that the coupling effect vanishes with time,
- $\phi'_{2,1}(s')$ is also proportional to the design gain K'_v and, therefore, choosing a value closer to zero has a benefit on avoiding the coupling between both axis,
- both terms $\phi'_{1,2}(s')$ and $\phi'_{2,1}(s')$ present the following zeros

$$z = \left\{ \frac{-K'_i}{b_d K'_p}, \frac{-K'_i}{b_q K'_p} \right\}, \tag{50}$$

that can be properly tuned depending on the controller gains K'_p and K'_i and weighting factors b_d and b_q.

With respect the last item, one must notice that the zeros in a transfer function imply an increase in the frequency response in middle frequencies. The lower the zeros values, the higher the amplification on medium frequencies. In order to decrease the coupling dq axis effects, is interesting to have higher zero values in (50). In the case of choosing the values $b_d = 0$ and $b_q = 0$ those zeros and their effects disappear, helping to diminish the coupling effect. Therefore, this is the best option to mitigate the coupling effects under weak grids, but one must take also into account that these values must be chosen also to face the destabilizing effects of the delays or the PLL.

4.3. Noise amplification

The measurements $v_{g_{dq}}$ and i_{dq} used by the controller to compute the control actions can be affected by high frequency noises that must be considered to avoid high frequency components in the applied voltages u_{dq}. The transfer functions that define the control actions are:

$$u_{dq}(s) = v_{g_{dq}}(s) + \left(C_d - C_y(s)\right) i_{dq}(s) + C_r(s)\, i^*_{dq}(s), \tag{51}$$

being $i^*_{dq}(s)$

$$i^*_{dq}(s) = H_S \begin{bmatrix} P^* \\ V_N \end{bmatrix} + H_V v_{g_{dq}}(s).$$

For evaluating the effect of those noises over the control, the noise frequency is approximated to infinite, and then, the transfer functions in (51) are evaluated on $s \to \infty$. Let us assume that the voltage and current measurements in dq terms have independent measurement noise signals for channels d and q, but both with the same variance values Σ_v^2 and Σ_i^2, respectively. Then, the variance of the control actions due to measurement noises are

$$\Sigma^2_{u_d} = \left(1 + \frac{2\, P^*_o\, b_d\, K_p}{3\, V^2_{g_o}}\right)^2 \Sigma_v^2 + \left(L_c^2 \omega_g^2 + K_p^2\right) \Sigma_i^2 \tag{52a}$$

$$\Sigma^2_{u_q} = \left(1 + (b_q\, K_v\, K_p)^2\right) \Sigma_v^2 + \left(L_c^2 \omega_g^2 + K_p^2\right) \Sigma_i^2 \tag{52b}$$

in which the dependence of these variances w.r.t the design parameters K_v, K_p, b_d and b_q can be observed. In fact, K_p appears in each of the terms related to controller parameters and, therefore, it can be stated that K_p is the main responsible of possible noise amplification.

4.4. Summary of the properties

With the previous analysis, if the converter parameters, the controller parameters and the grid inductance are known, it can be stated

- the maximum voltage and power deviation through (19) and (20).
- if the system is stable when facing weak grids after checking conditions (35)
- if the system can become unstable due to PLLs or measurement delays by checking conditions (41) and (42), or, if they are not fulfilled, by obtaining the delay margin in (40).
- the settling time in tracking power references in both weak and stiff grids by checking (45) and (47), respectively
- the actuator activity, and thus, the amount of high frequency components of the converter voltage signal through equations defined in (52).

Furthermore, if the controller parameters are known, it can be stated which is the maximum grid inductance that the converter can support using (36) and (37). In the expressions used to obtain the properties it can be seen that there are different controller parameters that present an influence in opposite directions, leading to some trade-off when deciding the controller parameter values:

- High K_p values lead to fast response under disturbances (see (43)), but at the same time lead to high measurement noise amplification (see (52)).
- High K_i values lead to fast response in reference tracking (see (45) and (47)), but, on the contrary, can lead to oscillatory responses (see (34)) and a reduction on the capacity to face weak grids (see limit in GS (36) and requirement (35b)).
- K_v should be negative to achieve lower voltage and power deviations, i.e., $K_v < 0$ and to suppress its influence on the achievable grid strength limit (see (35a) and (36)). Higher values in $|K_v|$ lead to lower voltage and power deviation, as well to higher robustness against weakness in the time response sense (see (46)) but, on the contrary, lead to worse behaviour to face the delays induced by the measurements and PLL (see Fig. 7).
- High $b_d K_p$ values lead to fast response in reference tracking (see (45) and (47) when assuming $K_v < 0$), but at the same time reduces the ability to cope with weak grids (see limit in GS (36) and requirement (35a)). Furthermore, high values of $b_d K_p$ lead to high measurement noise amplification (see (52a)).
- Assuming $K_v < 0$, $K_p > 0$ and $b_q > 0$, high $|b_q K_v K_p|$ values lead to increase the ability to cope with weak grids (see limit in GS (36) and requirement (35c)), but, on the contrary, lead to high measurement noise amplification (see (52b)).

5. Controller design proposal

5.1. Controller goals

As it can be seen, deciding the controller parameters is a trade-off problem between different desires regarding

- speed response,
- oscillatory behaviour,
- robustness against the weakness of the grid,
- robustness against the effects of the delays and the PLL,
- measurement noise amplification.

In this sense, several design procedures can be developed attending to the specifications to be guaranteed and the ones to be optimized. In this section it is presented our proposal to obtain the parameters of a controller as follows: given the parameters of the converter, the transformer and the grid (i.e., V_N, P_r, L_c, R_c and ω_g) and given the following desires:

- stable operation under very weak grids,
- maximum time response $t_s^\star$ under reference changes in the inner current control loop to track power references under stiff grids (nominal conditions),
- damping $\xi^\star$ of the closed loop poles of the inner current control loop in nominal conditions to avoid oscillatory behaviour,
- and a maximum allowed voltage deviation $v^*_{g_d}$ ($v^*_{g_d} < V_N$) when facing weak grids,

obtain the controller parameter values K_p, K_i, b_d, b_q and K_v to guarantee them and to maximize the robustness against delays produced by measurements or the PLL.

5.2. Controller design procedure

Then, in order to assure that the converter is able to face very weak grids, the design is focused on facing grids with $\mathrm{SCR}_N = 1$ in (7), i.e., it is assumed that the highest possible value of the grid impedance that must be faced is $X_g = Z_b$. Note that this value $\mathrm{SCR}_N = 1$ does not correspond to the finally achieved SCR, as will be seen later. However, facing the operation of grids with $X_g \leq Z_b$ allows reaching the capability of facing very weak grids.

With that assumption it can be stated from the steady state behaviour in (19) that the gain K_v required to assure $v^\star_{g_d}$ is

$$K_v = \frac{\frac{v^\star_{g_d}}{V_N}}{2\,Z_b\left(\frac{v^\star_{g_d}}{V_N} - 1\right)}, \tag{53}$$

that, as expected, is a negative value. In the case that the maximum allowable grid impedance is greater than Z_b, the previous value on K_v will lead to voltages higher than $v^\star_{g_d}$, thus, fulfilling the specification.

It is proposed now to fix

$$b_d = 0 \tag{54}$$

in order to assure the highest robustness against weak grids (see (36) and Fig. 5), the highest robustness against delays and the PLL (see distance to point −1 in Fig. 7), and in order to minimize the noise effects (see (52a)). Once $b_d = 0$ is fixed, expressions (34) and (47) can be used, as well as dimensionless expressions (28) to fix both K_i and K_p as

$$K_i = \frac{16\,L_c}{\left(\xi^\star\, t^\star_s\right)^2} \tag{55a}$$

$$K_p = -R_c + \frac{8\,L_c}{t^\star_s}. \tag{55b}$$

Finally, to fix b_q, several approaches can be considered. On one hand, one can choose $b_q = 0$ to minimize its effect over noise amplification. On the other hand, one can set $b_q = 1$ in order to maximize the robustness against weak grids as one can see in (36) and Fig. 5 taking into account that $K_v < 0$. Finally, another third option is to set the value of $b_q \in [0, 1]$ that leads to the highest DM in (40) through an optimization that, in this case, reduces to a search within the range $b_q \in [0, 1]$, what can be addressed through a simple gridding approach. These three approaches can be summarized as follows[5]

$$b_q = \begin{cases} 0, \text{ i.e., } \min\ (52b) \\ \arg\max_{b_q}\ \mathrm{DM}(\lambda(s'))\ (40) \\ 1, \text{ i.e., } \min\ \mathrm{GS}_{\min}\ (36) \end{cases} \tag{56}$$

5.3. Achieved robustness

Once K_p, K_i, b_d, b_q and K_v have been obtained, the real supportable weakness can be obtained as follows. First, the grid stiffness $\mathrm{GS}^0_{\min}$ is obtained using (36).

$$\mathrm{GS}^0_{\min} = \max\left\{0,\ \frac{L_c}{R_c}\frac{Z_b\,\omega_g\,b_q\,K_v\,K_p + K_i}{K_p + R_c}\right\} \tag{57}$$

where $b_d = 0$ and $K_v < 0$ have been considered. Then, as it has been considered that X_g value to be at most of Z_b (at least to compute K_v and fulfil the voltage requirement), the achievable grid impedance $X_{g,\max} = L_{g,\max}\,\omega_g$ is expressed as

$$X_{g,\max} = \min\{Z_b,\ \frac{L_c\,\omega_g}{R_c\,\mathrm{GS}^0_{\min}}Z_b\}. \tag{58}$$

Once the supportable maximum grid impedance is determined, the real maximum voltage deviation can be obtained with (19) (using K_v obtained from (53)) and the power deviation $P_{\max}$ with (20). With this value, the achievable SCR can finally be obtained as

$$\mathrm{SCR}_{\min} = \frac{3}{2}\,\frac{V_N^2}{X_{g,\max}\,P_{\max}}. \tag{59}$$

With the proposed approach, the problems to be faced by the controller have been mostly decoupled:

- achieving a desired steady state through K_v in (53),
- achieving a given closed loop dynamic performance through K_p and K_i in (55), and
- achieving a given robustness against delays, PLL bandwidth and grid weakness through b_d and b_q in (54) and (56).

Table 1
Parameters used in the simulations.

Parameter	Value	Parameter	Value
S_r	350 MVA	R_c	1.0864 Ω
V_N	159.2 kV	L_c	69.2 mH
Z_b	108.65 Ω	I_r	1.465 kA
$\omega_g/(2\pi)$	50 Hz		

6. Simulation results

This section is devoted to shown the simulations done with the Simulink toolbox SymPowerSystems. An average model based on fundamental frequency has been used for the modular multilevel converter [37]. Table 1 shows the values of the parameters of the electrical model used in these simulations.

6.1. Effect of the controller parameters

Table 2 shows the parameters of the controllers used in the different simulations. It is also shown the maximum weakness of the grid in terms of the maximum supportable grid inductance $L_{g,\max}$, and also the minimum SCR_N and $\mathrm{SCR}_{\min}$ using (59). There are also the PCC voltage values $\frac{v_{g_d}}{V_N}$ and the maximum derated power $\frac{P_{\max}}{S_r}$ evaluated at $L_{g,\max}$ value. In addition, Table 2 shows the settling times in nominal conditions t_s and $t_{s,dist}$ obtained with (43) and (47) respectively, the phase and delay margins of $\lambda(s')$ in (40) for the particular case in which $L_g = 173$ mH (equivalent to a $\mathrm{SCR}_N = 2$) and, finally, the term $(b_q K_v K_p)^2$ in (52b) related to the noise amplification.

Fig. 8 shows the behaviour of the three controllers C1.x defined in Table 2. They have been designed with the same values for the parameters K_p, K_i, K_v and b_q, and only differ in the b_d values. Note that, C1.1 is equivalent to the standard PI (i.e., $b_d = b_q = 1$) designed using an IMC ($K_p = \frac{L_c}{\alpha}$, $K_i = \frac{R_c}{\alpha}$)[6] with $\alpha = 1.7$ ms.

In this simulation, two step changes in L_g are provoked at 0.2 and 0.6 s and it can be seen that weaker grids can be faced thanks to lower b_d values in terms of higher grid impedances and SCR_N. However, there are also higher voltage drops and lower achievable power levels. This effect is considered in the computed $\mathrm{SCR}_{\min}$ shown in Table 2, and it can be observed that there is a minimum in the achievable $\mathrm{SCR}_{\min}$ for a value of $b_d = [0.55, 1]$. It is also worth mentioning that, for the same controller, lower values of b_d lead to higher settling times against reference step changes t_s.

Fig. 9 shows the behaviour of controllers C2.x defined in Table 2 when a step change in the power reference with $L_g = 173$ mH (equivalent to $\mathrm{SCR}_N = 2$) is provoked. In this case, three equal standard PI controllers with three different values for K_v are compared.

[5] $\mathrm{DM}(\lambda(s'))$ must be read as Delay Margin of transfer function $\lambda(s')$.

[6] In this case, $\phi^N_{1,1}(s) = \phi^N_{2,2}(s) = \frac{1}{1+\alpha\,s}$, i.e., the nominal closed loop dynamics is a first order system (non oscillatory) with unitary gain and constant time α leading to $t_{s,dist}$ and t_s equal to 4α.

Table 2
Controllers used in the simulations.

	K_p [Ω]	K_i [$\frac{\Omega}{s}$]	K_v [$\frac{1}{\Omega}$]	$Z_b K_v$ [–]	b_d [–]	b_q [–]	$L_{g,\max}$ [mH]	SCR_N [–]	$\text{SCR}_{\min}$ [–]	$\frac{v_{g_d}}{V_N}$ [p.u.]	$\frac{P_{max}}{S_r}$ [p.u.]	t_s [ms]	$t_{s,dist}$ [ms]	PM [deg]	DM [ms]	$(b_q K_v K_p)^2$ [–]
C1.1	40	628	0	0	1	1	188	1.84	2.2	0.84	0.84	6.9	13.5	∞	∞	0
C1.2	40	628	0	0	0.80	1	234	1.47	2.0	0.73	0.73	57.8	13.5	∞	∞	0
C1.3	40	628	0	0	0.55	1	342	1.01	6.6	0.15	0.15	121.5	13.5	∞	∞	0
C2.1	27.2	1279	−0.036	−4	1	1	277	1.25	1.44	0.92	0.87	3.4	19.6	76.5	1.5	1
C2.2	27.2	1279	−0.018	−2	1	1	277	1.25	1.50	0.86	0.82	3.4	19.6	133.4	11.4	0.25
C2.3	27.2	1279	−0.009	−1	1	1	277	1.25	1.62	0.79	0.77	3.4	19.6	∞	∞	0.06
C3.1	27.7	434	−0.009	−1	1	1	271	1.27	1.63	0.80	0.78	10	19.2	∞	∞	0.07
C3.2	27.7	434	−0.036	−4	1	1	271	1.27	1.46	0.92	0.87	10	19.2	78.8	1.5	1.04
C3.3	54.3	11 172	−0.036	−4	0.25	0.25	346	1	1.26	0.89	0.79	15	10	87.6	3.1	0.25
C4.1	35.8	9839	−0.053	−5.75	0	0	346	1	1.22	0.92	0.82	15	15	32.4	0.88	0
C4.2	35.8	9839	−0.053	−5.75	0	1	346	1	1.22	0.92	0.82	15	15	100.2	1.35	3.59
C4.3	35.8	9839	−0.053	−5.75	0	0.45	346	1	1.22	0.92	0.82	15	15	84.1	2.09	0.73

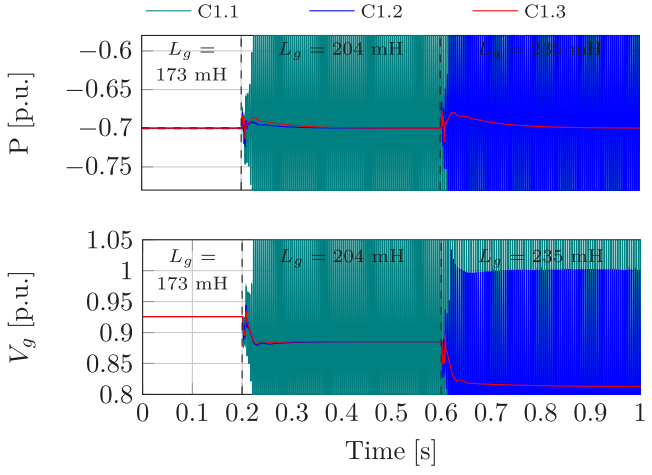

Fig. 8. Effect of the parameter b_d in the maximum achievable L_g. Controllers C1.x.

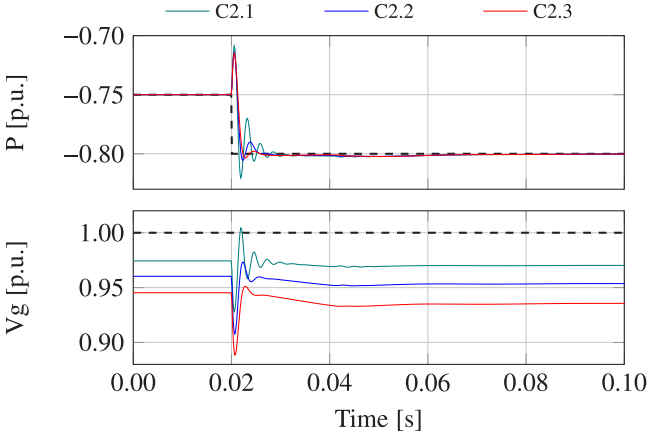

Fig. 9. Effect of the gain K_v on tracking power references (L_g = 173 mH). Controllers C2.x.

It can be seen that the more negative value for K_v, the smaller voltage droop w.r.t the nominal value. However, there is also a more oscillatory behaviour, which makes the system closer to the instability and higher noise amplification due to the term $(b_q K_v K_p)^2$ in (52b). This negative effect of using higher values of K_v in absolute value, can also be seen in the Nyquist diagram in Fig. 10, where it is shown that the more negative K_v, the lower DM.

Fig. 11 is devoted to validate the results obtained in Section 4.1 summarized in the Eqs. (19) and (20) and Fig. 3. In this simulation, a step change in the active power reference is provoked from −0.75 p.u.

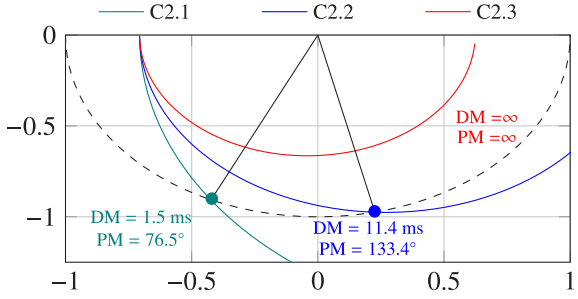

Fig. 10. Nyquist diagram of $\lambda(s')$ for controllers C2.x.

to −0.85 p.u. at 0.05 s and from −0.85 p.u. to −1 p.u. at 0.2 s and then a change in L_g from 173 mH to 216 mH at 0.35 s. Here, the controllers C3.x defined in Table 2 are compared. The controllers C3.1 and C3.2 are the same standard PI controllers (same K_p, K_i values, and $b_d = b_q = 1$) with different values of K_v. The C3.3 controller has different values of K_p, K_i, b_d and b_q compared to C3.1 and C3.2 but it has the same K_v value of the controller C3.2. As it is derived from (19) and (20), for a given grid impedance X_g, the steady state behaviour (i.e., the voltage drop $\frac{v_{g_d}}{V_N}$ and the maximum derated power $\frac{P_{\max}}{S_r}$), only depends on the K_v parameter. It can be observed that K_p, K_i, b_d and b_q only has an effect on the transient behaviour. Additionally, it can be observed (when the power reference is set to -1, p.u.) that it is not possible to operate at the nominal power (in absolute value) S_r, and that the maximum power value at which operation is feasible depends on the grid inductance L_g. The results shown in this simulation match those predicted by (19) and (20), as well as with Fig. 3.

6.2. Design proposal

In Fig. 12 the C4.x controllers defined in Table 2 are compared. C4.x controllers have been designed by using the design method proposed in Section 5 for achieving the following specifications:

- The settling time $t_s \leq 15$ ms.
- The damping $\xi \geq 0.707$.
- The PCC voltage $\frac{v_{g_d}}{V_N} \geq 0.92$ p.u.

The three C4.x controllers fulfil these specifications and have the same K_p, K_i, K_v and b_d parameters. They only differ in their b_q values. It can be observed the effect of the different values of b_q on the noise amplification (term $(b_q K_v K_p)^2$ in (52b)), i.e., lower values of b_q lead to a lower noise amplification, and that there is an optimum value when maximizing the maximum supportable DM for $b_q = 0.45$, as it is shown in Fig. 13. In the simulation in Fig. 12, it can be seen that it is not possible to operate at nominal power. However, the three controllers track power references (if the power reference do not exceed

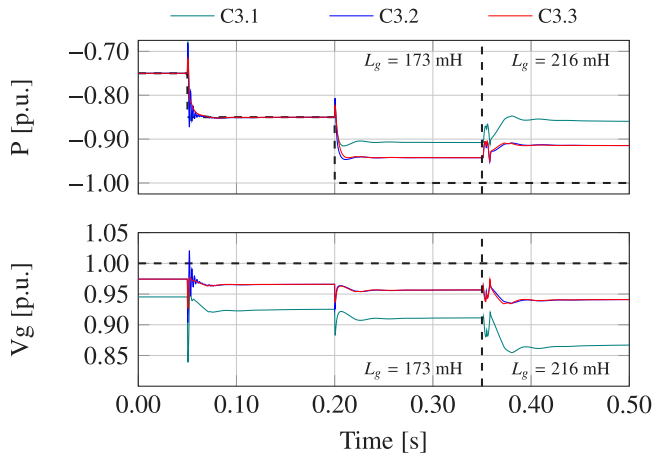

Fig. 11. Effect of the controller parameters and the grid inductance on the steady state behaviour. Controllers C3.x.

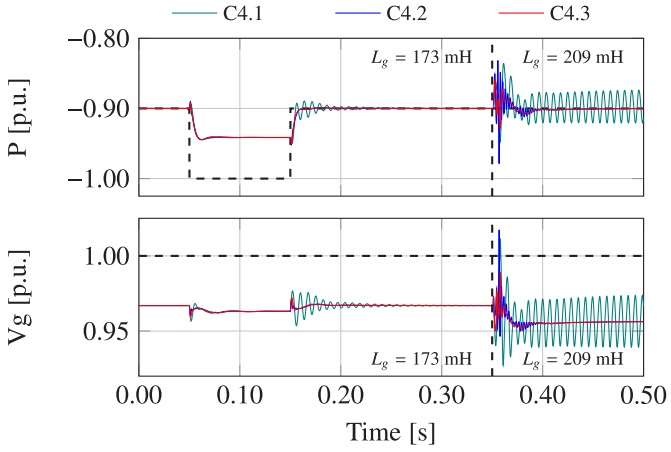

Fig. 12. Behaviour of the proposed controller design method. Controllers C4.x.

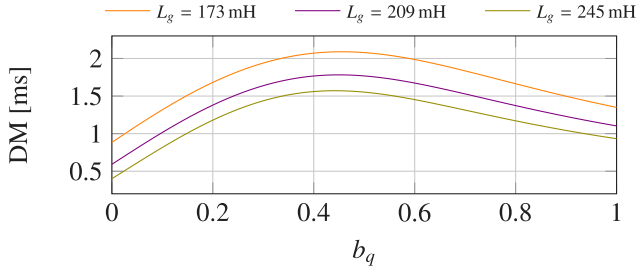

Fig. 13. DM as a function of b_q for C4.x controllers and different L_g values.

$P_{\max}$ defined in (20)) with different transient behaviours. It can also be observed that when the grid inductance L_g is increased from 173 mH to 209 mH, the effect of the delays and the interaction with the PLL also increase and the C4.1 controller, the one with lower supportable DM, becomes unstable.

6.3. Disturbance effects

In Fig. 14 it is shown for controllers C4.x, which is the effect of variations of $v_{x_{dq}}$ over the achieved power P and voltage, where those variations of $v_{x_{dq}}$ can be understood as disturbances for the control system. Two steps have been applied on this variable, of −0.05 p.u. and −0.30 p.u., at t=0.05s and t=0.35s respectively as depicted in the

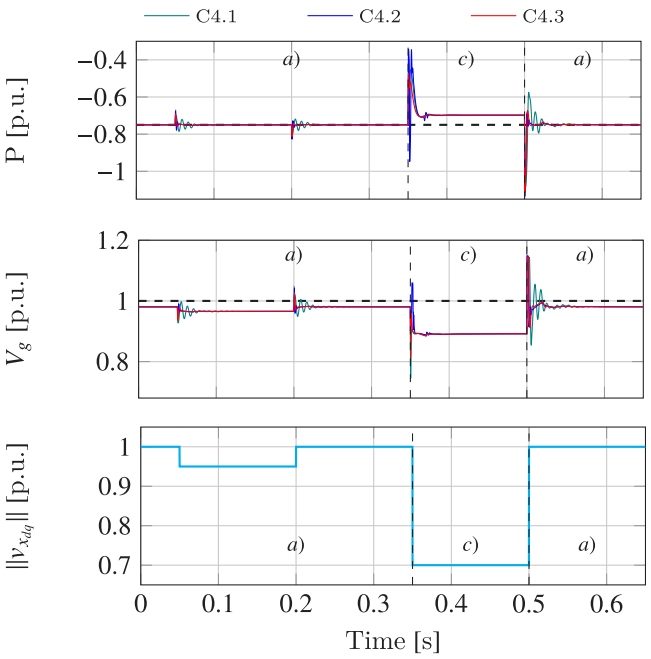

Fig. 14. Effect on P and V_g of disturbance $v_{x_{dq}}$ step changes. Controllers C4.x.

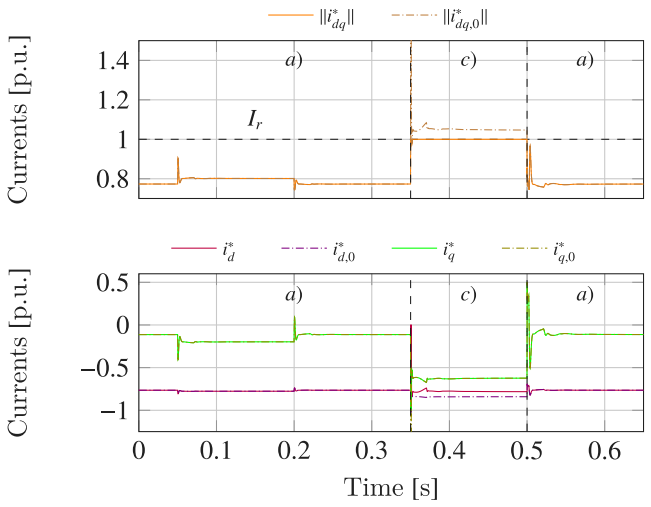

Fig. 15. Effect on the current references $i^*_{dq,0}$ and i^*_{dq} of disturbance $v_{x_{dq}}$ step changes. Controller C4.3.

bottom graph of Fig. 14. Here it can be seen, on the one hand, the coupling between the channels P and V_g. At steady state, the coupling is the same for the three controllers; however, the transient behaviour is different. In this sense, C4.3 is the one with the least coupling. On the other hand, it can be observed that for the first step change, the ability to track the power references is retained, but this ability is lost for higher disturbance step changes.

Fig. 15 shows the module of current references $i^*_{dq_0}$ and i^*_{dq} and the d and q components of these currents, only for case of the controller C4.3. In addition to the behaviour of the current references, in these two graphs it is indicated which of the four possible scenarios defined in Section 3.2 (i.e., (*a*), (*b*), (*c*) or (*d*), deduced from (14a) and (14b)) we are operating at each instant of time. Here, it can be observed that when the step of −0.30 p.u. is applied, voltage control is prioritized over power control, i.e., scenario (*c*) applies.

Fig. 16 shows for the controllers C4.x how a large variation on $v_{x_{dq}}$ (step change of −0.80 p.u.) affects power P and voltage V_g, and how the

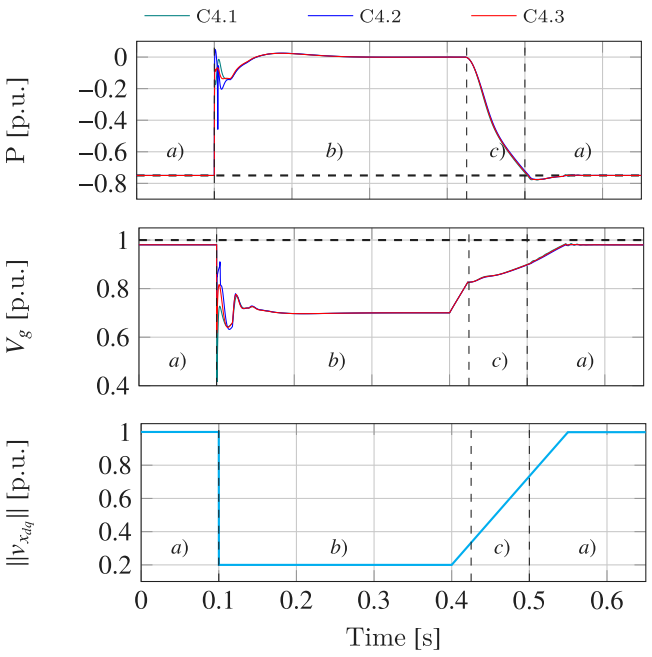

Fig. 16. Effect on P and V_g of a large disturbance. Controllers C4.x.

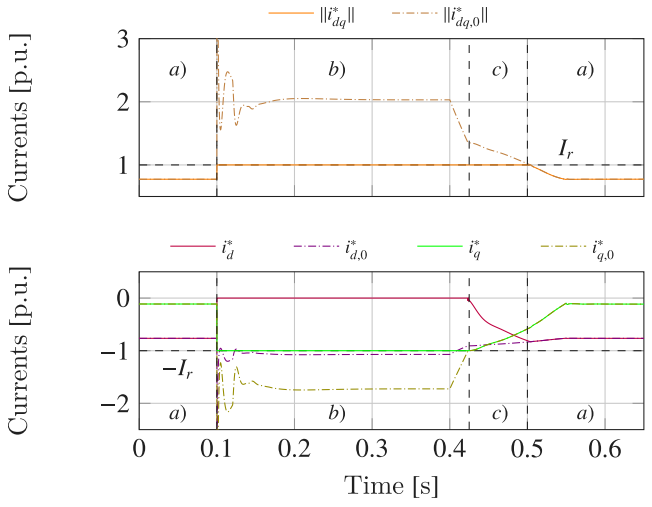

Fig. 17. Effect on the current references $i^*_{dq,0}$ and i^*_{dq} of a large disturbance. Controllers C4.3.

system is recovered after 300 ms (see bottom graph of Fig. 16). Here it can be seen that in case of a large disturbance, we move from scenario (a) to scenario (b) in which the active power exchanged P goes to zero while the voltage V_g drops to a particular level.

Fig. 17 shows the module of current references $i^*_{dq,0}$ and i^*_{dq} and the d and q components of these currents, only for case of the controller C4.3. In these graphs it can be seen that in the event of a large disturbance, the system is moved from scenario (a) to scenario (b) in which $|i^*_{dq,0}| > I_r$, $|i^*_{q,0}| > |i^*_q| = I_r$ and $|i^*_{d,0}| > |i^*_d| = 0$. It can also be observed that in the recovery process it is returned to scenario (a) from scenario (b) temporarily passing through scenario (c).

6.4. Coupling effects

Finally, it can observed in the different presented controllers, that the values b_d and b_q and K_v play a role on decreasing the coupling effect between dq axis and, in consequence, an effect on the coupling between the control of P and V_g. Fig. 9 shows that controller C2.3 (with lower K_v value w.r.t C2.1 and C2.2) presents a lower coupling effect. It can be seen in Fig. 11 that controller C3.3 presents a lower coupling effect than C3.1, where both share the same K_v value, but where C3.3 has lower values in b_d and b_q. Finally, Figs. 12, 14 and 16 where all the controllers C4.x have null values in b_d and the same K_v values, but different values in b_q, shows that b_q has an effect of mitigating the coupling effects, but its value must be correctly chosen to address also the compromise in allowing facing greater delay effects in the PLL.

Table 3
Predicted values in saturation conditions.

	L_g = 173 mH		L_g = 204 mH	
	v_{gd}	P_{max}	v_{gd}	P_{max}
C5	0.957	0.942	0.946	0.923
C6	0.866	0.866	0.808	0.808

6.5. Comparison on saturation alternatives

In this section the effect of using saturation mechanism (14) or (A.1) is discussed via simulations. As stated in the outer controller presentation (Section 3.2), this mechanism plays an important role when the current controls are saturated (*scenario c*).

Fig. 18 compares the performance of controller C3.3 when implemented with two different saturation mechanisms after the power and voltage controllers. C5 refers to the use of i_q prioritization (14), while C6 refers to i_d prioritization (A.1). Expressions (19) and (20), as well as (A.2) allow to predict voltage and power values depending on the grid inductance in saturation conditions, leading to the values shown in Table 3 for different L_g values below the stability limit $L_{g,max}$ = 346 mH.

Initially, with L_g = 173 mH, the active power reference is increased from 0.85 to 0.94 pu at t = 0.15 s. As a result, the active current increases and the voltage at the PCC (V_g) decreases. The voltage controller generates thus a higher $i^*_{q,0}$ current demand. In this case, simulation shows that these variations lead to a higher reactive power (Q) injection. The time response of both controllers is exactly the same given that none of them saturates. Under these conditions (P^* = 0.94 p.u.< P_{max} = 0.942 p.u.), the converter almost reaches the rated current and active power, i.e., saturation has still not occurred but about to do it if an increase in P^* or in L_g occurs.

Next, at t = 0.5 s the grid impedance increases to 204 mH, i.e., decreases the SCR, and decreases the maximum allowable power without saturations to P_{max} = 0.923 p.u, as well as the maximum PCC voltage to 0.946 p.u. In this case, the modulus of the current references obtained from the voltage control and active power control are higher than 1 p.u. as it can be observed in the bottom graph of Fig. 18 (dash-dotted lines). Therefore, the current references are saturated to 1 p.u. in modulus with their respective strategies. C6 (i.e., i_d prioritization) shows that the active current increases up to 1 pu trying to deliver the rated active power. However, the reactive current reduces to 0 p.u., due to controller saturation, which, in turn, reduces the reactive power injection and also the PCC voltage. Thus, given that no voltage support is provided, the PCC voltage drops to 0.808 p.u. and the maximum active power is 0.808 p.u., as predicted in Table 3, while the i_d and the i_q values are 1 p.u. and 0 p.u., respectively.

Conversely, for C5 (i_q prioritization), the PCC voltage remains much closer to its rated value. This allows to exchange up to 0.923 pu, even with a smaller active current (i_d = 0.975 p.u. and i_q = 0.22 p.u.). Due to the current saturation, the converter is not able to deliver its rated active power, however, the power reduction for C5 is much smaller than for C6, in which i_d is prioritized.

Note that the objective of the proposed control is to deliver the demanded active power. The prioritization of i_q or i_d only plays role in the case of current saturation, i.e., if the demanded current reference

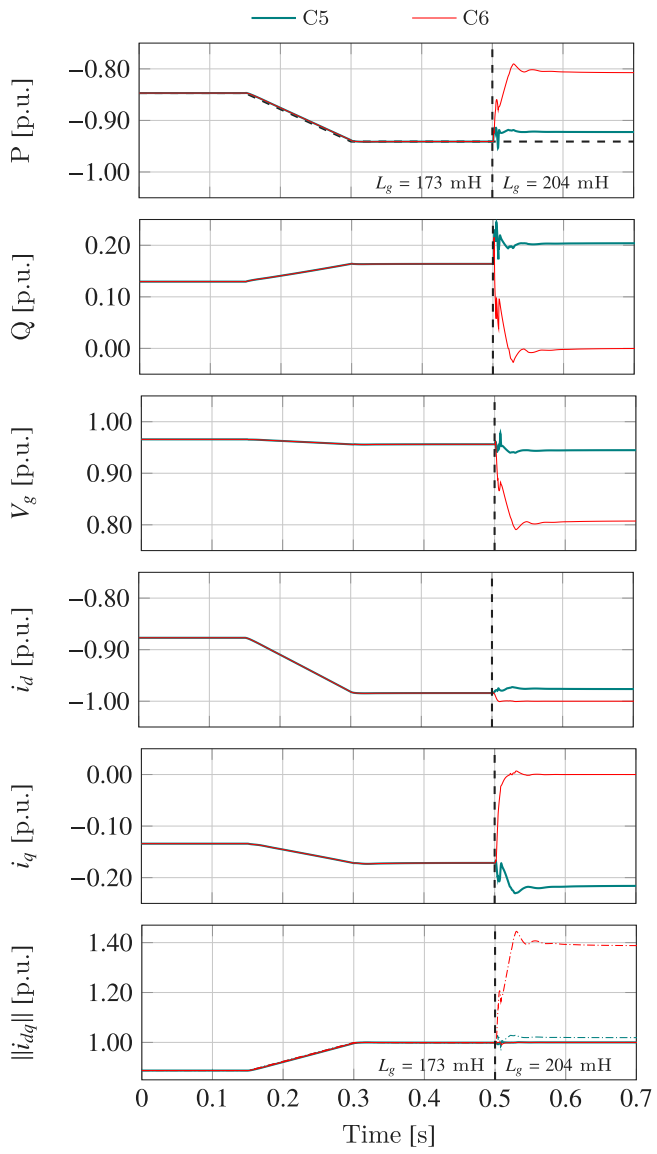

Fig. 18. Effect of saturation mechanism: C5 (with (14)) and C6 (with (A.1)). The dash-dotted lines in the bottom graph are the modulus of the current references without saturation $i^*_{dq,0}$.

by power and voltage controllers lead to a modulus that is higher than 1 p.u. If the saturation occurs, for instance for an eventually drop in the SCR, then, it has been shown and justified that it is better to prioritize i_q tracking through (14) than to prioritize i_d through (A.1), given that (14) allows to keep the PCC voltage closer to its rated value and, in consequence, deliver more active power.

7. Conclusions

In this work, the problem of power control of a VSC connected to a WG has been addressed. A control strategy has been proposed, based on making small changes to the conventional VCC structure, allowing connection to weaker grids. These changes include the use of 2DOF-PI controllers instead of standard PI controllers for the inner current control loop, the use of a P controller in the outer voltage control loop to maintain the voltage at PCC within specified limits, and a saturation mechanism that guarantees maximum power injection and minimum allowable short circuit ratio under weak grid operation. With this proposal, three more design parameters are introduced compared to the conventional VCC strategy. Additionally, a controller design method has been proposed, thanks to a normalization procedure and analytical analysis of the system, to guarantee specifications regarding maximum voltage deviations at PCC, minimum admissible SCR, time response, high-frequency behaviour, and maximum supported delays. This method allows for exploration of wider design areas for the controllers compared to conventional design strategies, such as those based on the IMC. Furthermore, our design procedure allows the design of each controller parameter to be related to given design goals related to steady state, dynamic performance, and robustness against grid weakness, delays, or PLLs. Therefore, through simulations, it has been shown that, thanks to the extra design parameters and the proposed design method, controllers can be obtained that achieve better behaviour in WG scenarios.

CRediT authorship contribution statement

Carlos Díaz-Sanahuja: Writing – review & editing, Writing – original draft, Visualization, Validation, Supervision, Software, Project administration, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Ignacio Peñarrocha-Alós:** Writing – review & editing, Writing – original draft, Supervision, Project administration, Methodology, Investigation, Funding acquisition, Formal analysis, Conceptualization. **Ricardo Vidal-Albalate:** Writing – review & editing, Writing – original draft, Investigation, Formal analysis, Conceptualization. **Agustí Egea-Àlvarez:** Writing – review & editing, Writing – original draft, Supervision, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Appendix. Saturation alternatives comparison

Another alternative approach to limit the demanded currents by the power and voltage controllers when they exceed the rated one I_r in modulus is to minimize the d current alteration over the q one as follows

$$i^*_d = \begin{cases} i^*_{d,0}, & \text{if} \quad -I_r \le i^*_{d,0} \le I_r \\ \text{sgn}(i^*_{d,0})\, I_r, & \text{otherwise} \end{cases} \tag{A.1a}$$

$$i^*_q = \begin{cases} i^*_{q,0}, & \text{if } i^{*2}_d + i^{*2}_{q,0} \le I^2_r \\ \text{sgn}(i^*_{q,0}) \sqrt{I^2_r - i^{*2}_d}, & \text{otherwise} \end{cases} \tag{A.1b}$$

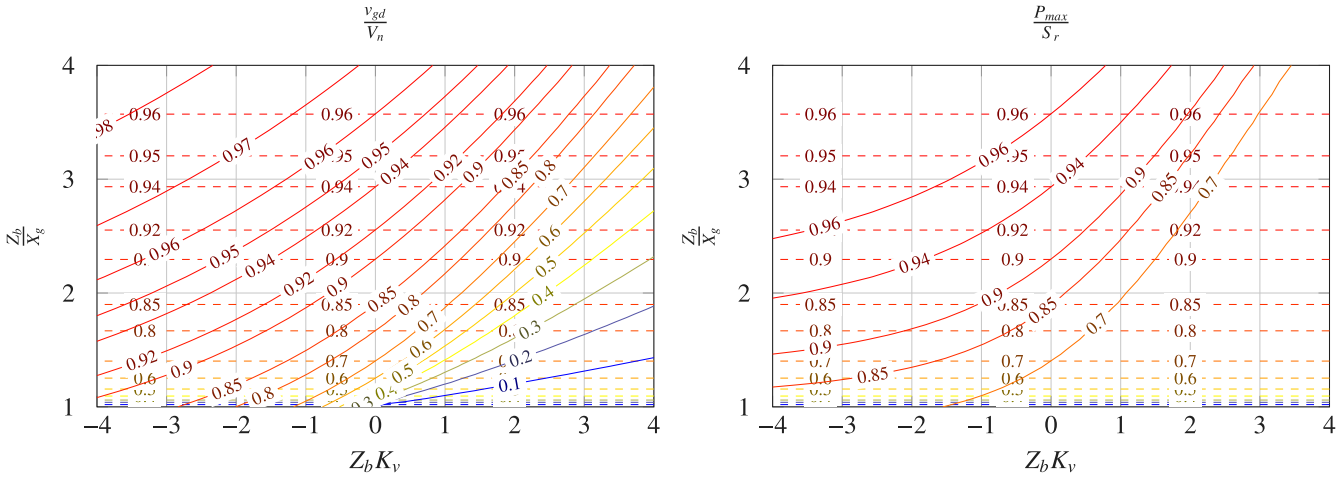

Fig. A.19. $\frac{v_{gd}}{V_n}$ levels at PCC as a function of $\frac{Z_b}{X_g}$ and $Z_b K_v$. Saturation prioritizing i_d (dashed line), saturation prioritizing i_q (solid line).

When this saturation strategy is applied, the steady state values for voltage and power (19) and (20) become

$$\frac{v_{g_d}}{V_N} = \frac{\sqrt{\left(\frac{Z_b}{X_g}\right)^2 - 1}}{\frac{Z_b}{X_g}}, \qquad \frac{P_{max}}{S_r} = \frac{v_{g_d}}{V_N}, \tag{A.2}$$

which do not depend on K_v. Fig. 3 shows these values in dashed lines. It can be observed that, for a particular expected grid weakness and a controller defined by K_v, it is possible to exchange higher active powers if saturation (14) is applied, i.e., preferring achieving the demanded q current over the d one, as it is proposed in this work. Similarly, for a specific gain K_v in the voltage controller and a given desired active power, the proposal of prioritizing i_q (14) enables operation at lower values of SCR_N w.r.t. strategy (A.1).

Finally, another intermediate alternative approach would be to limit both currents but keeping the initially computed angle, that is

$$i_d^* = \begin{cases} i_{d,0}^*, & \text{if} \quad {i_{d,0}^*}^2 + {i_{q,0}^*}^2 \le I_r^2 \\ \frac{i_{d,0}^*}{\sqrt{{i_{d,0}^*}^2 + {i_{q,0}^*}^2}} I_r, & \text{otherwise} \end{cases} \tag{A.3a}$$

$$i_q^* = \begin{cases} i_{q,0}^*, & \text{if } {i_{d,0}^*}^2 + {i_{q,0}^*}^2 \le I_r^2 \\ \frac{i_{q,0}^*}{\sqrt{{i_{d,0}^*}^2 + {i_{q,0}^*}^2}} I_r, & \text{otherwise} \end{cases} \tag{A.3b}$$

As the values of d and q currents lie between the achievable ones w.r.t. the other two analysed alternatives, the resulting achievable power and voltage drop lies also between the previous results. Therefore, the alternative of minimizing the q current deviation when alterations are needed is the best option to fulfil both, high power and low voltage drop.

Appendix B. Supplementary data

Supplementary material related to this article can be found online at https://doi.org/10.1016/j.ijepes.2024.110120.

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