Efficient model for modular multi-level converter simulation

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Abstract

Detailed models of modular multi-level converters (MMCs) are cumbersome for electromagnetic transient simulation programs because of their high number of components which involve large simulation times. In this work, the modeling of an MMC is addressed with the objective of reducing the simulation time. First, the MMC structure is presented, including the modulation technique, the voltage balancing algorithm and the circulating current control used to validate the model. Next, an efficient simplified model is proposed. This is formed by just one variable voltage source, one variable capacitor and one variable resistor per arm, regardless of the number of submodules. This simplified model allows the simulation time to be reduced while keeping the dynamics of the MMC. The comparison through several PSCAD simulations with a detailed 5-level MMC model proves its validity during both steady-state and transient conditions (ac and dc short-circuits).

Keywords: Modular multi-level converter (MMC), modeling, circulating current control, voltage source converter (VSC), simulation.

1. Introduction

Modular multi-level converters (MMCs) are a promising technology since they present a modular structure and provide a high voltage dc link [13], being therefore valid for their use in high voltage direct current (HVDC) grids, STATCOMs, railway traction systems, etc. [12, 17]. Most of the major worldwide power electronics manufacturers such as Siemens, ABB and Alstom are offering this technology nowadays [7, 4, 3].

It is therefore necessary to build accurate MMC models to analyze their operation, especially during faulty transient conditions, and to develop new control strategies. When used in high power and high voltage applications, the converters may have hundreds of levels which implies the modeling of thousands of components [5]. Detailed models include all the components but their complexity and simulation times increase enormously as the number of levels goes up. For that reason, only models with a low number of levels are typically considered in the analysis of the MMCs [22, 6].

Different models have been reported in the literature to overcome the aforementioned problem. Their level of accuracy and speed depends mainly on the model adopted for the IGBTs and the diodes [21]. Average-value models (AVMs) employ controlled voltage and current sources to represent the arm voltages and the dc side current respectively [16]. These models are very efficient computationally since the IGBTs are not explicitly represented and, in addition, they assume that all the inner variables (such as capacitor voltages or circulating current) are perfectly controlled. AVMs based on switching functions take into account the IGBT switching and, hence, the harmonics, whereas AVMs based on fundamental frequency only consider fundamental frequency components [15, 23]. The main limitation that these models present is their inability to simulate dc-side transients as well as to represent the internal converter dynamics. Therefore they may only be appropriate for steady-state, fundamental frequency studies.

More elaborated models have been built to represent MMCs faithfully. In [8] an equivalent-circuit-based model (based on a“nested fast and simultaneous solution” algorithm) is used to develop a Thevenin equivalent model for the converter. However, it was not verified during dc faults.

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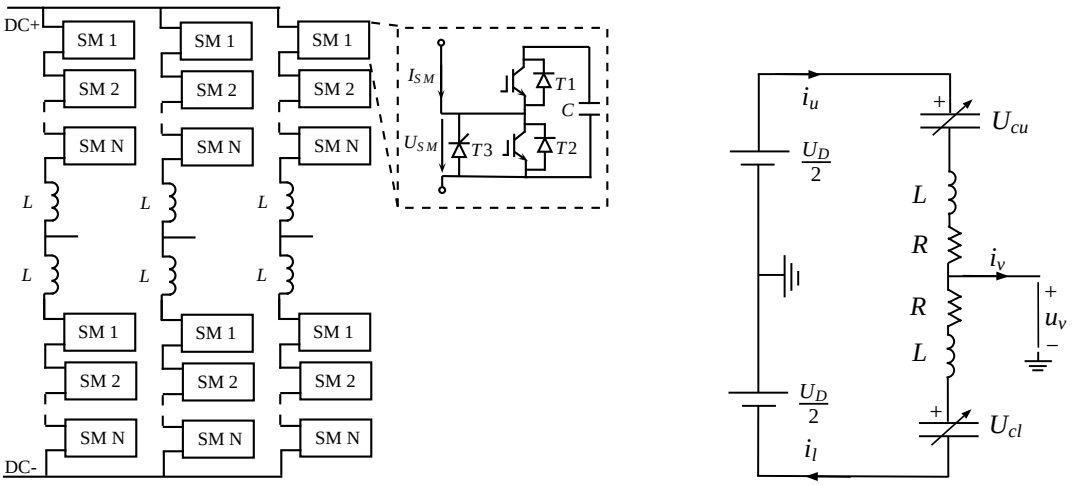


(a) Structure of the MMC.

(b) Equivalent circuit for one phase.

Figure 1: Modular multi-level converter.

An exhaustive comparison of all the aforementioned models is done in [20]. AVMs offer accurate results for steady state operation but not for transient situations. Equivalent-circuit-based models work properly for ac faults but appreciable differences appear during the simulation of dc faults.

Other models have been proposed to specifically simulate MMCs during transients, e.g., in [14] a reduced model based on an RLC circuit is used to evaluate the first transient after a dc fault.

So far, none of the reported simplified models is able to properly describe the MMC behavior under every type of conditions (steady state, ac and dc short-circuits). In this paper a new simplified and computationally efficient MMC model, based on a Thevenin equivalent circuit for each arm [26], is proposed for both steady state and transient conditions (ac and dc short-circuits). The behavior of MMCs during dc faults is thoroughly analyzed and some modifications are proposed in order to adapt the basic model to reproduce these conditions. Moreover, unlike AVMs, all inner variables such as capacitor voltages and arm currents are available so the proposed simplified model can be used instead of detailed models to validate different control strategies such as capacitor voltage balancing algorithms [9, 25] or circulating current controls [2, 1, 18].

2. Modular multi-level converter description

The basic structure of the MMC is shown in Fig. 1a. It consists of three legs, each one having an upper and a lower arm. Each arm is composed of N identical half-bridge series-connected submodules (SMs) and a reactor L, which is included to control the circulating current and to limit fault currents. Usual values of the arm reactors are around 0.10 - 0.15 p.u. [16]. Capacitor voltages are in the range of 1-5 kV and the stored energy is between 30-40 kJ/MVA [16, 11]. All the SMs also include a thyristor ($T3$) which is fired in the event of a dc line-to-line fault to protect the endangered diodes [7].

During normal operation, each submodule has two possible states: inserted (ON) or bypassed (OFF). It is considered to be ON when the upper IGBT/diode (T_1) is conducting. On the contrary, the cell is OFF when the lower IGBT/diode (T_2) is conducting. The SM is blocked when both IGBTs are switched off.

An equivalent circuit for one leg is shown in Fig. 1b. The voltages that have to be inserted in the upper and lower arm (U_{cu} and U_{cl}) of one phase are [1]:

$$U_{cu} = \frac{U_D}{2} - u_v - R\, i_u - L\frac{di_u}{dt} \tag{1a}$$

$$U_{cl} = \frac{U_D}{2} + u_v - R\, i_l - L\frac{di_l}{dt} \tag{1b}$$

where i_u is the current in the upper arm; i_l, the current in the lower arm; u_v, the output ac voltage and U_D, the pole-to-pole dc voltage. R is the parasitic arm resistance.

The Thevenin equivalent circuit of the MMC is obtained when subtracting the above two equations [24]

$$u_v = \frac{U_{cl} - U_{cu}}{2} - \frac{R}{2}\,(i_l - i_u) \;-\; \frac{L}{2}\frac{d}{dt}(i_l - i_u) = e_v - \frac{R}{2}\,i_v \;-\; \frac{L}{2}\frac{di_v}{dt} \tag{2}$$

where i_v is the output ac current and e_v is the internal converter voltage, i.e., the voltage that the MMC generates by controlling the voltages inserted in the upper and lower arms. Hence, the output current i_v can be controlled by means of e_v when the MMC is connected to an ac grid of voltage u_v.

Ideally, for a three-phase MMC, each arm would carry half of the ac output current plus a circulating current whose value should correspond to a third of the dc current. However, capacitor voltage variations lead to additional circulating current components in addition to the dc component that increase the rms value of the arm currents, the capacitor voltage oscillations and the overall losses.

The equivalent circuit for the circulating current is obtained when adding the equations in (1):

$$\frac{U_D}{2} = \frac{U_{cu} + U_{cl}}{2} + Ri_c + L\frac{di_c}{dt} \tag{3}$$

where i_c is the circulating current with a value of:

$$i_c = \frac{i_u + i_l}{2} \tag{4}$$

Note that the term $(U_{cu} + U_{cl})/2$ can be used to control the value of the circulating current.

2.1. Modulation strategy

To date, several modulation strategies have been proposed to drive MMCs. Some of them are based on pulse-width modulation (PWM) techniques such as: phase disposition (PD), alternative phase opposition disposition (APOD), phase opposition disposition (POD) or phase-shifted carrier PWM (PS-PWM) [10]. The voltage references for U_{cu} and U_{cl} are compared with N carrier signals to determine the number of submodules to insert in the upper and lower arms. Among them, note that the APOD method is the one used in this work.

2.2. Capacitor voltage balancing algorithm

The capacitor voltage balancing algorithm used in this work is based on the capacitor voltage measurements and the arm current direction [25]. If a new submodule is to be inserted and the arm current is positive (charging the capacitor), the algorithm chooses the SM in the OFF state that has the lowest capacitor voltage. If the current is negative, (discharging the capacitor), the mechanism selects the SM in the OFF state that has the highest voltage. Conversely, if a new SM is to be bypassed and the arm current is positive, the algorithm chooses the SM in the ON state that has the highest capacitor voltage. If the current is negative, the mechanism selects the submodule in the ON state that has the lowest voltage. This strategy allows for a low switching frequency as only one submodule changes its state every time the modulator ask for a switching operation.

2.3. Circulating current control

The open-loop control proposed in [1] is used to control the circulating current. According to Eq. 3, the circulating current can be controlled using the first term on the left-hand side of the equation. A proportional controller surveilling the voltage drop across the arm impedance, u_c^{ref}, is used to modify the inserted arm voltages (U_{cu} and U_{cl}) and, therefore, to control the circulating current:

$$u_c^{ref} = R_a(i_c^{ref} - i_c) + \widehat{R}i_c^{ref} \tag{5}$$

where R_a is referred as the "active resistance" and $\widehat{R}$ is an estimate of R. i_c^{ref} is the circulating current reference. Hereinafter i_c^{ref} is taken as the dc component of the circulating current. More details about its implementation can be found in [9].

Hence, the voltages to be inserted in each arm are [1]:

$$U_{cu} = \frac{U_D}{2} - e_v^{ref} - u_c^{ref} \tag{6a}$$

$$U_{cl} = \frac{U_D}{2} + e_v^{ref} - u_c^{ref} \tag{6b}$$

where e_v^{ref} is the reference voltage to be generated by the MMC.

3. MMC models

A new efficient and simplified model is proposed in this section. To prove its validity, it is compared with a fully detailed 5-level MMC model which is also introduced here. Note that although the comparison is with a 5-level model, the simplified model proposal is general and can be applied to substitute any MMC regardless of its number of levels.

3.1. Detailed model

The detailed model used in this work comprises all the components shown in Fig. 1a [16]. It has 4 submodules per arm and each SM consists of one capacitor, two IGBTs, the fly-wheeling diodes and a thyristor for protection purposes. An inductor, L, is also included in each arm. The modulation technique, the capacitor voltage balancing algorithm and the circulating current control implemented in this model are those presented in section 2.

This model is assumed to represent the dynamics of the MMC accurately according to previous works [20], and it is used here to validate the proposed simplified model.

3.2. Simplified model

The simplified model, based on the equivalent circuit, is shown in Fig. 2. As already introduced, it aims to reduce the computational requirements of the detailed models. As it can be observed in the figure, the simplified model consists of a variable voltage source, a variable capacitor, a variable resistor, and a reactor for each arm. Thus, all the SMs in each arm are reduced to these components, regardless of the considered number of levels.

The proposed simplified model is based on the Thevenin equivalent circuit with the following considerations:

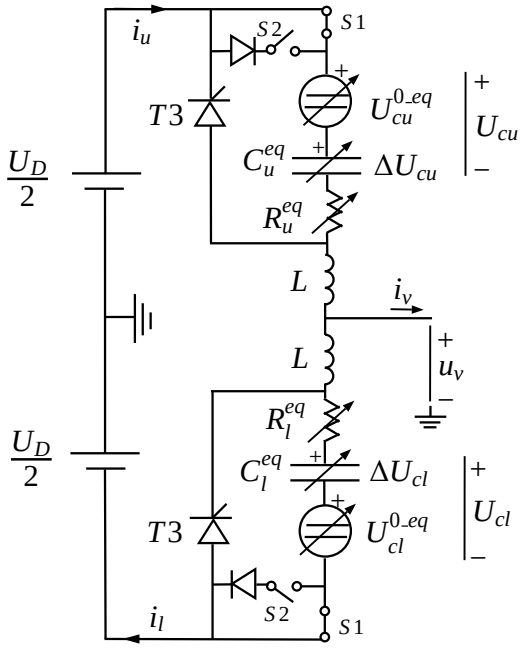


Figure 2: Equivalent circuit of one phase.

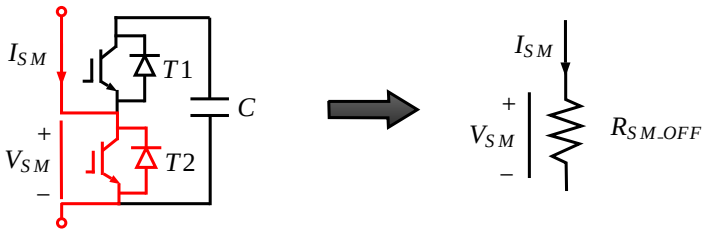


Figure 3: Equivalent circuit of an off-state submodule.

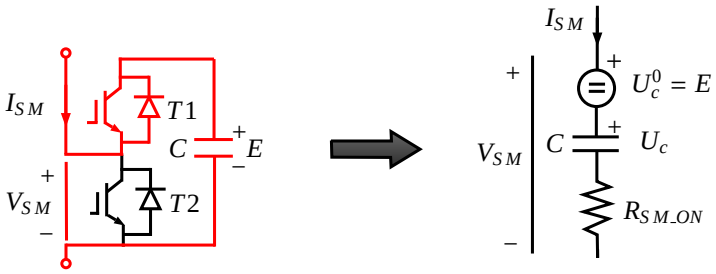


Figure 4: Equivalent circuit of an on-state submodule.

- **Consideration 1:** The IGBTs and diodes are modeled as a two-state resistance: R_{ON} and R_{OFF}.
- **Consideration 2:** The off-state resistance, R_{OFF}, of the IGBTs and diodes is considered to be infinite.
- **Consideration 3:** The off-state submodules are replaced by an equivalent resistor, R_{SM_OFF}, whose resistance is (see Fig. 3):

$$R_{SM\_OFF} = R_{ON}^{IGBT} \quad if \quad I_{SM} > 0 \tag{7a}$$

$$R_{SM\_OFF} = R_{ON}^{diode} \quad if \quad I_{SM} < 0 \tag{7b}$$

  where R_{ON}^{diode} and R_{ON}^{IGBT} are the diode and IGBT conduction resistance respectively.

  If there are N_{OFF} submodules in the OFF state, the equivalent resistance will be

$$R_{SM\_OFF}^{eq} = N_{OFF}\, R_{SM\_OFF} \tag{8}$$

- **Consideration 4:** The on-state submodules are replaced by an equivalent resistor, R_{SM_ON}, a capacitor, C, and a voltage source (see Fig. 4). The value of the resistance is:

$$R_{SM\_ON} = R_{ON}^{diode} \quad if \quad I_{SM} > 0 \tag{9a}$$

$$R_{SM\_ON} = R_{ON}^{IGBT} \quad if \quad I_{SM} < 0 \tag{9b}$$

  The value of the voltage source, U_c^0, is the capacitor voltage at the instant of time when the SM is connected. C is the capacitance of the cell capacitor. The initial voltage of the capacitor, U_c, is set to zero as its voltage has already been considered within the voltage source.

  If there are N_{ON} ($N_{ON} = N - N_{OFF}$) submodules in the ON state, the equivalent voltage source, resistance and capacitance will be:

$$R_{SM\_ON}^{eq} = N_{ON}\, R_{SM\_ON} \tag{10a}$$

$$U_c^{0\_eq} = \sum_{i=1}^{N_{ON}} U_c^0 \tag{10b}$$

$$C^{eq} = \frac{C}{N_{ON}} \tag{10c}$$

Note that only the on-state submodules are considered in the summation of eq. 10b.

To implement the above simplified model the following steps are run within the control code for each simulation step.

- **Step 1**: The voltages that have to be inserted in each arm at instant k ($U_{cu}(k)$ and $U_{cl}(k)$) are calculated by using (6). For the sake of simplicity, from now on, the upper and lower variables will be denoted together, e.g., $U_{cu,l}(k)$.

- **Step 2**: The modulation strategy determines the number of submodules to be connected in each arm at instant k, ($N_{u,l}(k)$).

  The following steps are only executed if a new SM has to be inserted or bypassed, i.e., $N_{u,l}(k) \neq N_{u,l}(k-1)$.

- **Step 3**: The total capacitor voltage increase of all inserted SMs in the upper and lower arm ($\Delta U_{cu,l}(k)$) is measured (see Fig. 2) and the capacitor voltage of each submodule at instant k, $U^i_{cu,l(SM)}(k)$, is calculated according to:

$$U^i_{cu,l(SM)}(k) = U^i_{cu,l(SM)}(k-1) + S^{\,i}_{u,l}(k-1)\frac{\Delta U_{cu,l}(k)}{N_{u,l}(k-1)} \tag{11}$$

  where $U^i_{cu,l(SM)}(k-1)$ is the capacitor voltage of the submodule i at instant $k-1$. $S^{\,i}_{u,l}$ is a binary variable that returns the state of the submodule i. Its value is 1 when the submodule is inserted and 0 when the submodule is bypassed.

- **Step 4**: The voltage balancing algorithm is implemented to select which specific submodule has to be inserted or bypassed. The vector containing the submodule states for each arm ($S_{u,l}(k)$) is updated.

- **Step 5**: The new values of the upper and lower capacitance are calculated.

$$C^{eq}_{u,l}(k) = \frac{C}{N_{u,l}(k)} \tag{12}$$

- **Step 6**: The new values of the equivalent variable voltage sources are computed.

$$U^{0\_eq}_{cu,l}(k) = \sum_{i=1}^{N} S^{\,i}_{u,l}(k) U^i_{cu,l(SM)}(k) \tag{13}$$

- **Step 7**: The new values of the equivalent resistances are determined.

$$\text{If} \quad i_{u,l} > 0:$$
$$R^{eq}_{u,l}(k) = R^{diode}_{ON} N_{u,l}(k) + R^{IGBT}_{ON}(N - N_{u,l}(k)) \tag{14a}$$
$$\text{If} \quad i_{u,l} < 0:$$
$$R^{eq}_{u,l}(k) = R^{diode}_{ON}(N - N_{u,l}(k)) + R^{IGBT}_{ON} N_{u,l}(k) \tag{14b}$$

  Here only the conduction losses are considered. However, the switching losses could be calculated off-line by means of the characteristic curve of the IGBT module as in [19]. Then, a parallel resistor from the positive to the negative pole can be added in order to take into account these switching losses.

- **Step 8**: The values of the variable voltage sources, the capacitances and resistances used in the simplified model are updated. The capacitor voltages are set to zero.

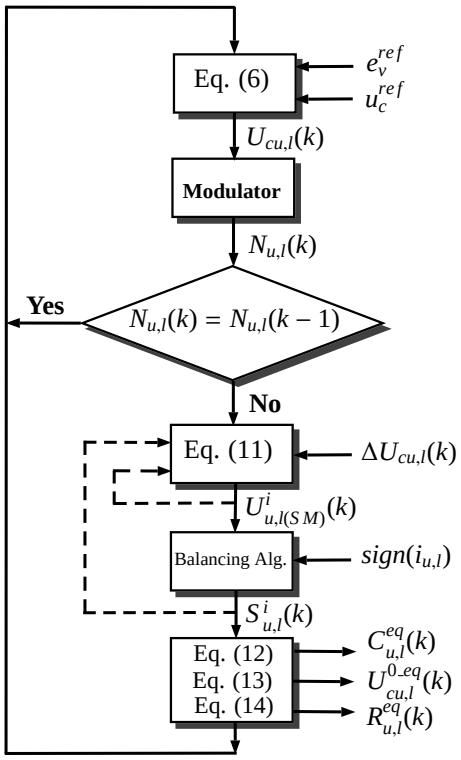


Figure 5: Flow chart for the simplified model.

The flow chart of the process is shown in Fig. 5. Note that the simplified model also provides all inner variables such as submodule capacitor voltages, upper and lower arm currents or circulating current.

The above model works properly for steady-state conditions, power flow changes and ac faults as it will be demonstrated in the results section. However, some modifications are required to take into consideration dc faults. When a dc fault occurs the thyristors $T3$ included in each cell are fired to avoid damaging overcurrents flowing through the fly-wheeling diodes. Once the protecting thyristors are fired, the converter works as an uncontrolled rectifier. To take into account this behavior the thyristor $T3$ is also included in each arm of the simplified model. They are fired in the event of a dc fault and at the same time the ideal switches *S1* are opened. Moreover, the following issues are considered to achieve a consistent behavior during faults:

- During a dc fault, large currents can flow through the SM capacitors if the protective thyristors are not fired. Therefore, capacitor voltages might become negative. As this is impossible due to the presence of the fly-wheeling diodes of $T2$, MMC cells will be considered to be OFF when their capacitor voltage reaches zero.

- When the thyristors $T3$ are triggered and the IGBTs $T1$ and $T2$ are switched off, the MMC becomes an uncontrolled rectifier. At each instant only one upper arm and one lower arm of the three phase MMC will be conducting in the case of a pole-to-pole fault. However, if the submodule capacitors are discharged, the diodes of $T1$ of the non-conducting arms can be forward biased. As a result current will flow through them until the capacitors are charged to a voltage that will depend on the MMC dc terminal voltage during the dc fault. An ideal diode and the switch *S2* are added to the simplified model in order to reproduce this characteristic (see Fig. 2).

  When the dc fault protection is triggered, i.e., the thyristors $T3$ are fired, the switches *S1* are opened and the switches *S2* are closed in the simplified model (see Fig. 2). In this way, the behavior of the actual MMC during the fault is accurately considered in the simplified model.

  The thyristors are modeled in the same way as the diodes, i.e., as two-state resistance where the off-state

resistance is infinite. To obtain adequate results, the $T3$ equivalent on-resistance will be the parallel of the on-state resistances of the diode and the thyristor:

$$R_t^{eq} = N \frac{R_{ON}^{diode} R_{ON}^{thyristor}}{R_{ON}^{diode} + R_{ON}^{thyristor}} \tag{15}$$

where R_t^{eq} is the on-state thyristor resistance used in the simplified model, R_{ON}^{diode} is the on-state diode resistance and $R_{ON}^{thyristor}$ is the on-state resistance of the thyristors used in the detailed model.

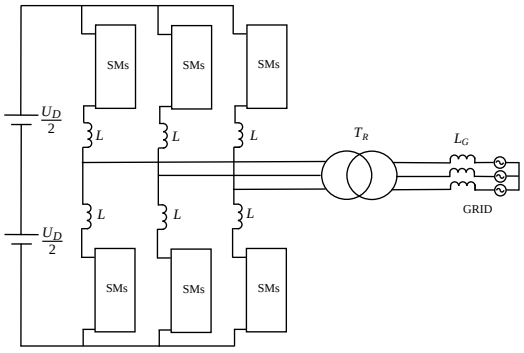
4. Results

4.1. Detailed and simplified 5-level MMC models

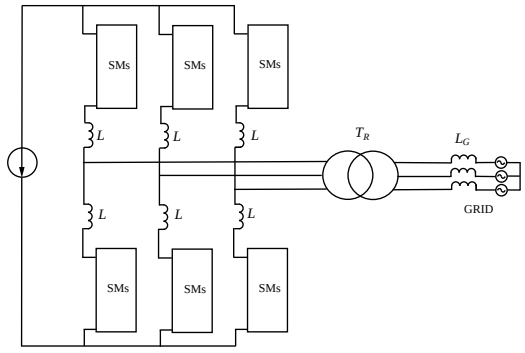
The three-phase simplified and detailed models are compared by means of PSCAD simulations with the goal of proving the accuracy and validity of the simplified model. To do that, power reference changes, ac faults, and dc faults are simulated. The system model is shown in Fig. 6 and the data for both MMC models are presented in Table 1. For power reference changes and ac faults simulation, the ac side of the MMC is connected to a 33 kV ac grid through a step up transformer ($R = 1.089\ \Omega$ and $L = 41.6$ mH, referred to the high voltage side) and the dc side is connected to a 6 kVdc voltage source (see Fig. 6a). For dc faults simulation, the dc side of the MMC is connected to a dc current source and the MMC is responsible for keeping the dc voltage constant (see Fig. 6b). The control of the converter is formed by two nested loops: an inner loop which controls the current in the d-q frame, and an outer loop that provides the current reference to the inner one according to the active and reactive power references or the dc voltage control loop.

4.1.1. Power reference changes

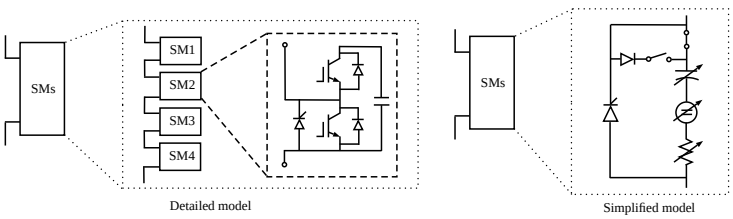
At $t = 0.5$ s the reference for the active power is stepped up from 0 to 3 MW as shown in Fig. 7c. The output voltage, u_v, and the output current, i_v, of one phase of both models are plotted in Fig. 7a. Fig. 7d shows the difference



(a) System model used for power reference changes and ac faults simulation.



(b) System model used for dc faults simulation.



(c) Arm representation for each model.

Figure 6: System model.

Table 1: Three-phase 5-level MMC data.

Number of levels ($N+1$)	5
Arm inductance (L)	1.3 mH
IGBT ON resistance (R_{ON}^{IGBT})	1 mΩ
Diode ON resistance (R_{ON}^{diode})	0.5 mΩ
Capacitor voltage (U_c)	1.5 kV
Capacitance (C)	7.4 mF
DC link voltage (U_D)	6 kV
Rated power	5 MW

Table 2: THD of the output voltage and current.

Output voltage (detailed model)	31.47 %
Output voltage (simplified model)	31.62 %
Output current (detailed model)	4.73 %
Output current (simplified model)	4.80 %

between the output current (with an amplitude of 1 kA) of the detailed and simplified models, with a standard deviation of 0.0052 kA.

Fig. 7b shows the upper and lower arm currents and the upper arm SM capacitor voltages of one phase. Note that the capacitor voltages of the simplified model are only updated when a new SM is inserted or bypassed in order to speed up the simulation.

The circulating current is shown in Fig. 8. At $t = 1$ s the control described in section 2.3 is enabled and the ac components of the circulating current are removed.

The THD of the output voltage and current for both models is presented in Table 2. Note how very similar results are obtained from both models.

4.1.2. Three-phase AC faults

A three-phase fault in the ac grid is simulated in this part. The ac voltage drops to 0.3 p.u. at $t = 1.5$ s while the active power reference is kept constant (for this test no current limits have been considered). Fig. 9 shows that the simplified model is able to reproduce accurately the system behavior during the transient.

4.1.3. DC pole-to-pole faults

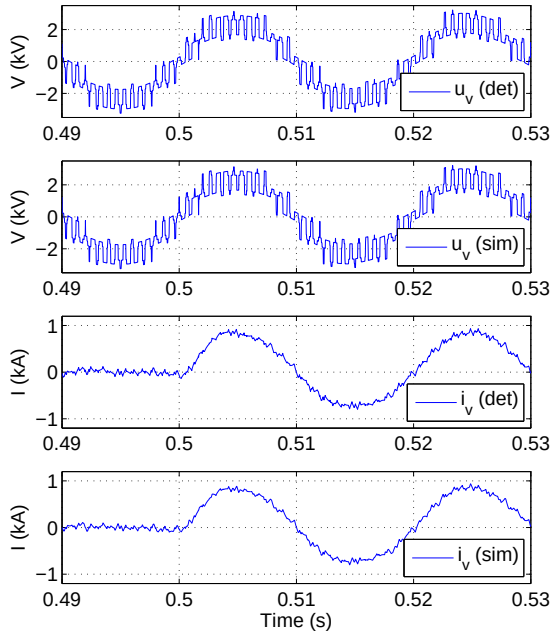
At $t = 2$ s a dc fault occurs and at $t = 2.05$ s the protection system of the submodules is enabled, i.e., the thyristors are fired. The results for both models are shown in Fig. 10.

The protections are not triggered during the first 50 ms to prove that the model also reproduces accurately the MMC behavior in those conditions. Due to the high currents, capacitor voltage oscillations are very large reaching zero volts in some cases, as previously mentioned. After firing the thyristors the capacitors are charged if they were discharged as in the case of the lower arm capacitors (see Fig. 10d). Afterwards their voltages remain constant.

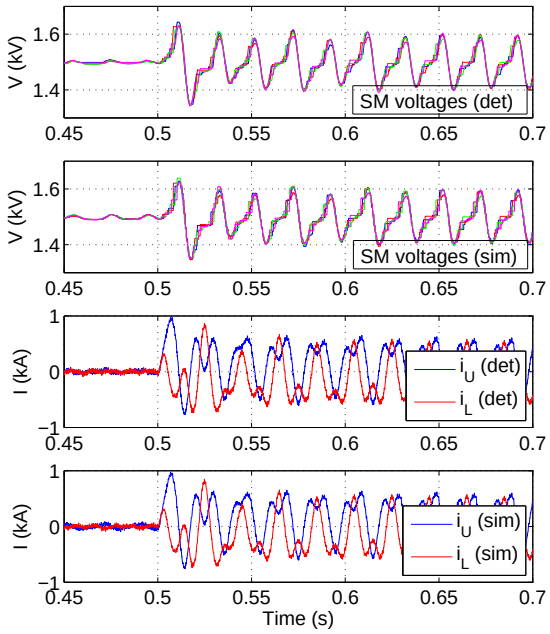
The minor differences observed when the capacitor voltages reach zero are due to the transient between the conduction of the IGBTs and the diodes. Additionally, the forward voltage drop of the diodes have not been considered either.

4.2. Simplified 151-level MMC

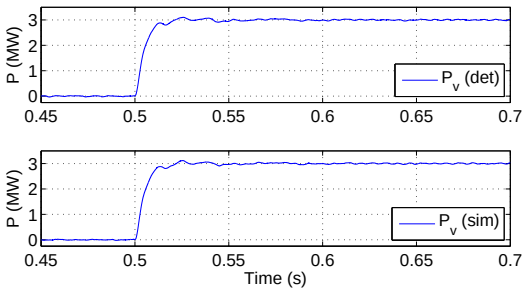
The simplified model has been scaled to a 151-level MMC and the previous simulations have been repeated. The data of this model are presented in Table 3. For power reference changes, the ac side of the MMC is connected to a 400 kV ac grid through a step up transformer ($R = 4\ \Omega$ and $L = 152$ mH, referred to the high voltage side) and the dc side is connected to a 300 kV dc voltage source (see Fig. 6a). For the dc faults simulation, the dc side of the MMC is connected to a dc current source as in the case of the 5-level MMC. (see Fig. 6b).



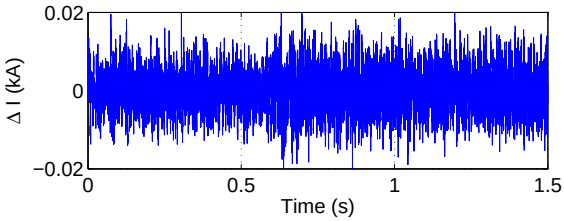
(a) Output voltage and current.



(b) Upper SM voltages and upper and lower arm currents.



(c) Output power.



(d) Output current difference between the detailed and simplified models.

Figure 7: Comparison of the simplified and detailed models during a step change in the active power reference

Table 3: Three-phase 151-level MMC data.

Number of levels ($N+1$)	151
Arm inductance (L)	25 mH
IGBT ON resistance (R_{ON}^{IGBT})	1 mΩ
Diode ON resistance (R_{ON}^{diode})	0.5 mΩ
Capacitor voltage (U_c)	2 kV
Capacitance (C)	8.9 mF
DC link voltage (U_D)	300 kV
Rated power	400 MW

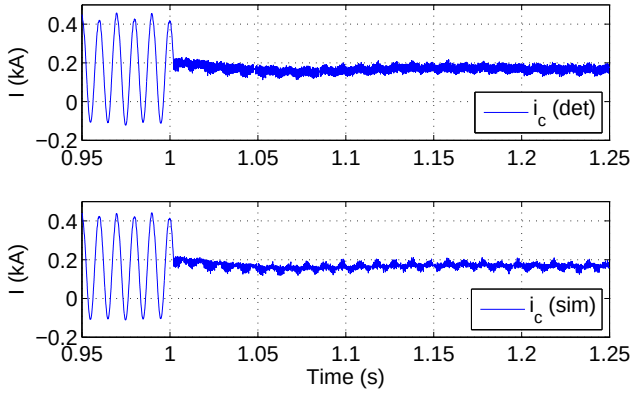
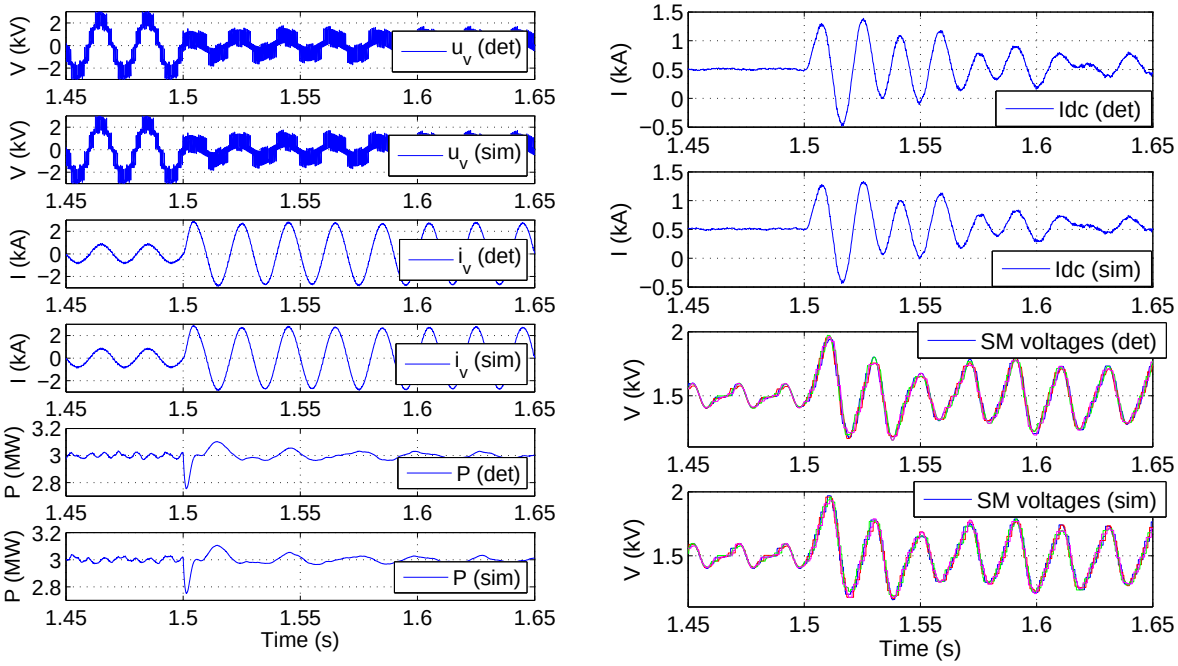


Figure 8: Comparison of the circulating currents.



(a) Output ac voltage, current and power.

(b) DC current and upper SM voltages.

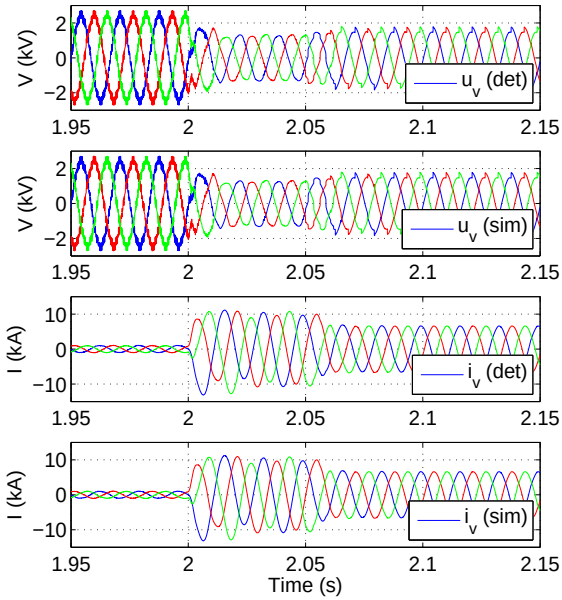
Figure 9: Comparison of the simplified and detailed models during an ac fault.

4.2.1. Power reference changes

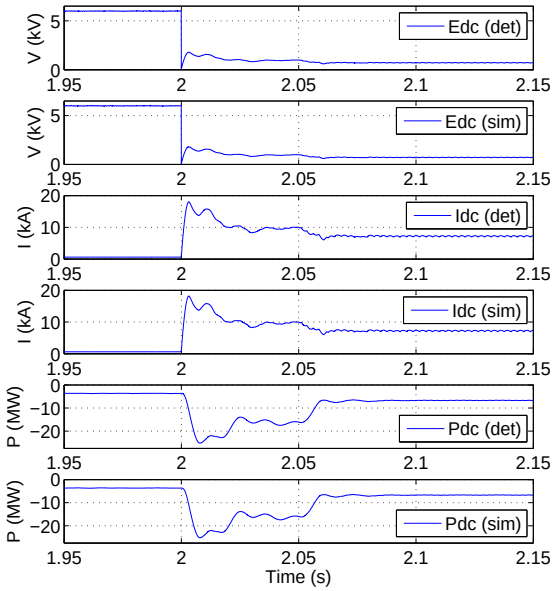
The power reference is ramped up from 0 to 400 MW at $t = 0.05$ s. The response to the power change is shown in Fig. 11. Note that in Fig. 11c only the average capacitors voltage of each arm is plotted for the sake of clarity, however, the voltages of all capacitors are available as in the case of the 5-level MMC.

4.2.2. DC pole-to-pole faults

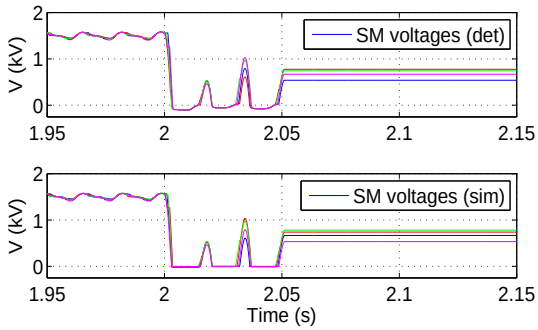
Finally, the dc side has been connected to a dc current source as in subsection 4.1.3. The dc load is 150 MW and the MMC is responsible for controlling the dc voltage. At $t = 0.05$ s a dc fault occurs and the protections are fired 2 ms later. The response of the simplified model is shown in Fig. 12.



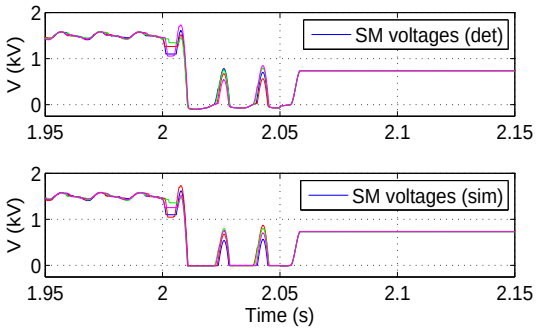
(a) Output voltage and current.



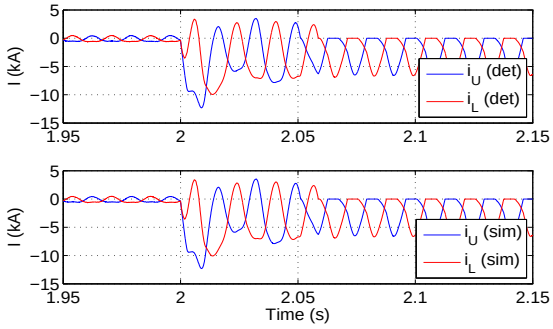
(b) DC voltage, current and power.



(c) Submodule voltages of the upper arm of phase a.

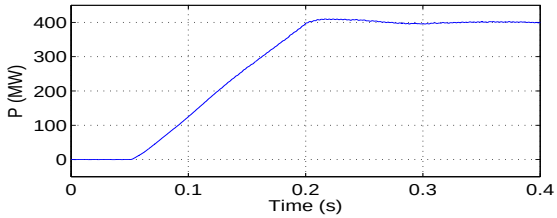


(d) Submodule voltages of the lower arm of phase a.

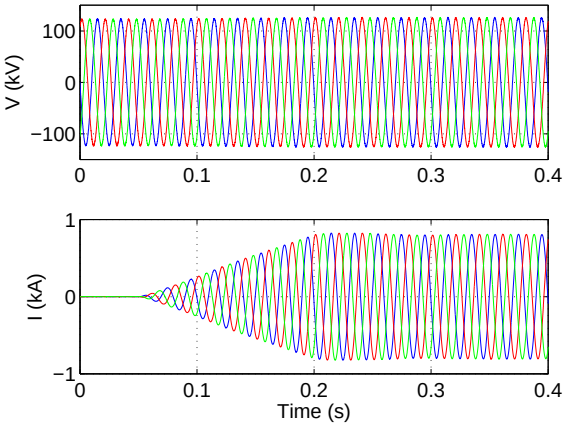


(e) Arm currents.

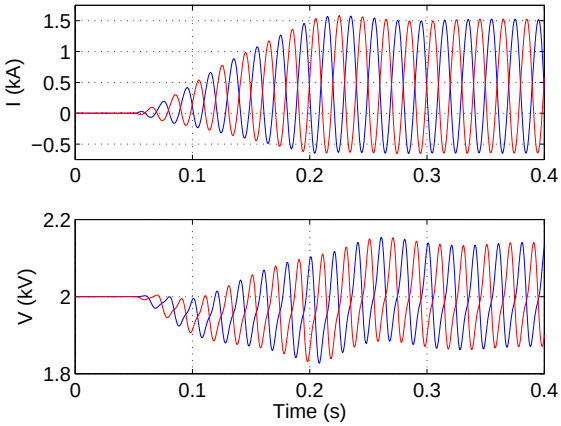
Figure 10: Comparison of the simplified and detailed models during a dc fault.



(a) Output power.

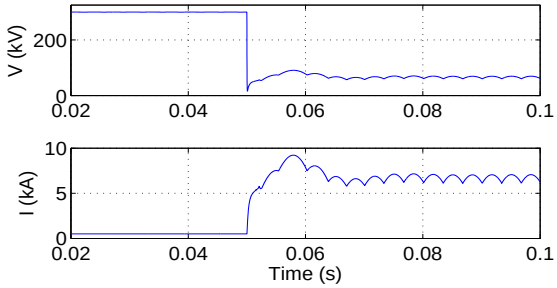


(b) Output voltage and current.

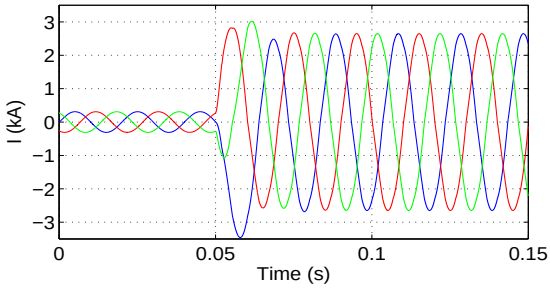


(c) Arm currents and average capacitors voltage of phase a.

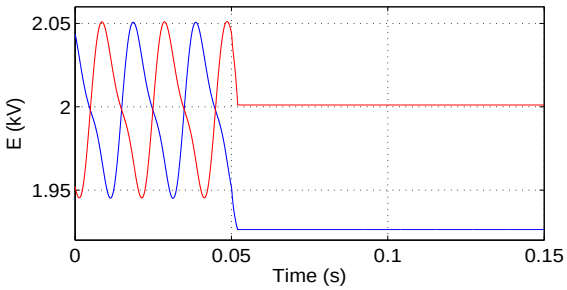
Figure 11: Response to a power reference change of the 151-level MMC model.



(a) DC voltage and current.



(b) AC current.



(c) Average capacitors voltage of phase a.

Figure 12: Response to a dc fault of the 151-level MMC model.

Table 4: Computing times.

Simulation step (μs)	20	40
5-level detailed MMC model (s)	260	210
5-level simplified MMC model (s)	16	10
Simulation step (μs)	5	10
151-level simplified MMC model (s)	72	38

4.3. Simulation efficiency

The simulations were made on a Microsoft Windows 7 platform with a 3GHz Intel Core i5, 4 GB of RAM running PSCAD version 4.2. The integration method used is the one included in PSCAD, i.e., Euler integration plus chattering correction. Table 4 tabulates the CPU times for the proposed simplified model and for the detailed one for two different simulation steps. A 10 s period was simulated in every case. The proposed simplified model leads to a 20 fold decrease in simulation time for a 5-level MMC. The simplified 151-level MMC only leads to a four fold increase in simulation times over the 5-level simplified MMC, mainly due to the lower simulation step required.

5. Conclusions

This paper has presented a simplified model that allows an efficient and accurate simulation of modular multi-level converters (MMCs) during both, steady-state and transient conditions. Special attention has been paid to the response to ac and dc short-circuits. All the submodules of each arm are replaced by a voltage source, a capacitor, and a resistor regardless of the number of levels, so the proposed solution reduces the simulation time while it keeps the dynamics of the MMC and makes available all the inner functioning variables.

The model is flexible and can be easily scaled. It only needs information about the number of levels of the converter to represent, the capacitance of the capacitors included in the converter's submodules, the on-state resistance of the diodes and the IGBTs used in the converter, and the arm inductance. A standard capacitor balancing strategy and a circulation current control method have been used in this paper but other control techniques could be implemented with the proposed simplified model.

The simplified model has been verified against a detailed model of the converter which included all the individual devices actually conforming it. The accuracy and validity of the proposal has been proven for both steady state and transient operation modes, showing the results scarce differences among the models behavior. Moreover, the proposed model lead to a 20 fold decrease in the simulation time for a 5-level MMC.

Finally, results for a simplified 151-level MMC have also been included, with just a four fold increase in simulation time with regard to that required for the 5-level simplified MMC.

Acknowledgements

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